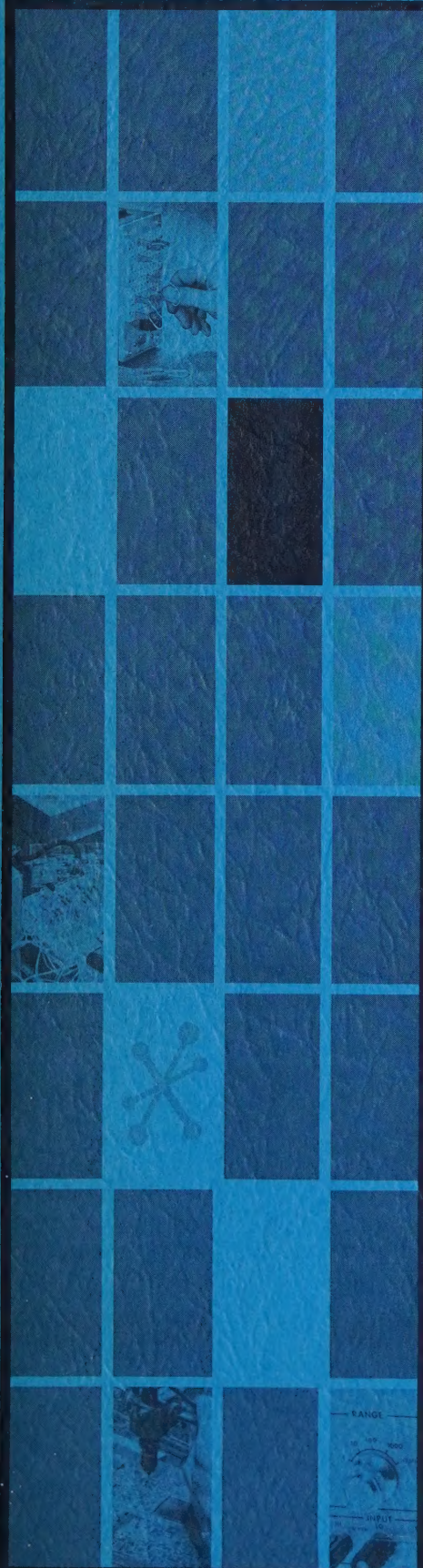


Joe COTOIA



PRESTON

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TRAINING MANUAL TMX7901

FOR MODEL GMAD1 ANALOG-DIGITAL CONVERSION SYSTEM
PART NUMBER 58885

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SHADY ANALOG TO DIGITAL CONVERTER UNIT CONSISTS OF TWO UNITS
PART NUMBER 33700-12
WHICH CONTAINS:

INTRODUCTION

THIS MANUAL CONTAINS SOME INFORMATION SPECIFICALLY DEVELOPED FOR TRAINING PURPOSES WHICH IS NOT RELEASED AS STANDARD DOCUMENTATION FOR THIS SYSTEM. IT IS BELIEVED TO BE ACCURATE AND IN AGREEMENT WITH DRAWINGS APPLICABLE TO THIS SYSTEM BUT IF DIFFERENCES DO EXIST THE RELEASED DOCUMENTS SHALL BE CONSIDERED CORRECT.

1 EACH MODEL 39-3 CARD MODULE WITH POWER SUPPLY
40 CH MODEL 39-3 MULTIPLEVER
36 CH MODEL 39-3 AMPLIFIER-MULTIPLEVER

THE OPERATION AND MAINTENANCE MANUAL CONTAINS A COMPLETE LIST OF ALL DRAWINGS APPLICABLE TO THIS SYSTEM.

INTRODUCTION

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THE OPERATION AND MAINTENANCE MANUAL CONTAINS A COMPLETE LIST OF ALL DRAWINGS APPLICABLE TO THIS SYSTEM.

SYSTEM DESCRIPTION

*** SYSTEM COMPONENTS ***

GMAD1 ANALOG TO DIGITAL CONVERSION SYSTEM CONSISTS OF TWO UNITS.
PART NUMBER 58700-XX WHICH CONTAINS:

1 EACH: MODEL GMAD1-15B A/D CONVERTER
1 EACH: MODEL GMSH-10 SAMPLE-AND-HOLD
1 EACH: MODEL GMC-RFL-LOGIC CONTROL SYSTEM
4 CH : MODEL GMD AMPLIFIER-MULTIPLEXER
16 CH : MODEL GMM MULTIPLEXER
1 EACH: ZERO CROSSING CONTROL CIRCUIT
1 EACH: MODEL GM-2 CARD MODULE WITH POWER SUPPLY

PART NUMBER 58845-XX
WHICH CONTAINS:

1 EACH MODEL GM-3 CARD MODULE WITH POWER SUPPLY
40 CH MODEL GMM-D MULTIPLEXER
36 CH MODEL GMD AMPLIFIER-MULTIPLEXER
GUARD DRIVERS AND SUB-MUX

*** SYSTEM COMPONENTS ***

GMADI ANALOG TO DIGITAL CONVERSION SYSTEM CONSISTS OF TWO UNITS.
PART NUMBER 58700-XX
WHICH CONTAINS:

MODEL GMADI-15B A/D CONVERTER	1 EACH:
MODEL GMSH-10 SAMPLE-AND-HOLD	1 EACH:
MODEL GMC-RFL-LOGIC CONTROL SYSTEM	1 EACH:
MODEL GMD AMPLIFIER-MULTIPLEXER	4 CH:
MODEL GMM MULTIPLEXER	16 CH:
ZERO CROSSING CONTROL CIRCUIT	1 EACH:
MODEL GM-S CARD MODULE WITH POWER SUPPLY	1 EACH:

PART NUMBER 58845-XX
WHICH CONTAINS:

MODEL GM-3 CARD MODULE WITH POWER SUPPLY	1 EACH:
MODEL GMM-D MULTIPLEXER	40 CH:
MODEL GMD AMPLIFIER-MULTIPLEXER	36 CH:
GUARD DRIVERS AND SUB-MUX	

SYSTEM DESCRIPTION

THIS SYSTEM (P/N 58885) CONSISTS OF TWO CHASSIS AND INTERCONNECT CABLES. THE FIRST CHASSIS CONTAINS THE A/D CONVERTER, MULTIPLEXER CHANNELS 0 >>>> 19 AND THE MULTIPLEXER CONTROL SYSTEM. THE EXPANSION CHASSIS CONTAINS MULTIPLEXER CHANNELS 20 >>> 55 AND 64 >>> 103, ASSOCIATED SUB-MULTIPLEXERS, AND LOGIC BUFFERS.

THIS SYSTEM WAS CONFIGURED TO MEET THE REQUIREMENTS OF
HAC SPECIFICATIONS: 258389 REV B
258392 REV D

SYSTEM DESCRIPTION

THIS SYSTEM (P/N 5882) CONSISTS OF TWO CHASSIS AND INTERCONNECTED CABLES. THE FIRST CHASSIS CONTAINS THE A/D CONVERTER, MULTIPLEXER CHANNELS 0 >> 19 AND THE MULTIPLEXER CONTROL SYSTEM. THE EXPANSION CHASSIS CONTAINS MULTIPLEXER CHANNELS 20 >> 35 AND 64 >> 103. ASSOCIATED SUB-MULTIPLEXERS AND LOGIC BUFFERS.

THIS SYSTEM WAS CONFIGURED TO MEET THE REQUIREMENTS OF
SPECIFICATION: 5882A REV B
5882B REV D

TERMINOLOGY

THE FOLLOWING TERMINOLOGY AND/OR ABBREVIATIONS ARE USED THROUGHOUT THIS MANUAL.

ADC	ANALOG-TO-DIGITAL CONVERTER
DAC	DIGITAL-TO-ANALOG CONVERTER
MUX	MULTIPLEXER (REFERS TO ANY TYPE IN THIS SYSTEM)
FET	N CHANNEL J-FET
COUNT	1 BIT CHANGE IN DIGITAL OUTPUT
S-H	SAMPLE-AND-HOLD
TRANSITION PT	AN OUTPUT CODE EITHER 12.5 OR 19.5 COUNTS FROM A MAJOR BIT COUNT.
TRANSITION WIDTH	A COMPARISON OF ACTUAL VOLTAGE ACROSS A TRANSITION COMPARED TO THE THEORETICAL VALUE
GND	ANALOG OR DIGITAL GROUND. NOT CONNECTED TO CHASSIS GROUND
A1	AMP-LOGIC CARD IN SLOT A-03 (SIGN)
A2	AMP-LOGIC CARD IN SLOT A-05 (8192)
A3	AMP-LOGIC CARD IN SLOT A-06 (4096)
A4	AMP-LOGIC CARD IN SLOT A-07 (2048)
A5	AMP-LOGIC CARD IN SLOT A-08 (1024)
A-B	AMP-LOGIC CARD IN SLOT A-09 (512)
B1	AMP-LOGIC CARD IN SLOT A-10 (256)
B2	AMP-LOGIC CARD IN SLOT A-11 (128)
C1	AMP-LOGIC CARD IN SLOT A-12 (64)
C2	AMP-LOGIC CARD IN SLOT A-13 (32)
C3	AMP-LOGIC CARD IN SLOT A-14 (16)
CALIBRATOR	EXTERNAL PRECISION SOURCE
JUMP	DIFFERENCE IN OUTPUT LEVELS OF S-H FOR THE SAMPLE AND HOLD TIMES.
MANUAL	OPERATION AND MAINTENANCE MANUAL FOR P/N 58855 SYSTEM
FET-MUX	GMM MULTIPLEXER (FET SWITCH ONLY)
AMP-MUX	GMD AMPLIFIER-MULTIPLEXER
CALIBRATION COVER	PRESTON PART NUMBER 52308 OR 52309 AS REQUIRED

TERMINOLOGY

THE FOLLOWING TERMINOLOGY AND/OR ABBREVIATIONS ARE USED THROUGHOUT THIS MANUAL.

ANALOG-TO-DIGITAL CONVERTER	
DIGITAL-TO-ANALOG CONVERTER	
MULTIPLEXER (REFERS TO ANY TYPE IN THIS SYSTEM)	
N CHANNEL J-FET	
1 BIT CHANGE IN DIGITAL OUTPUT	
SAMPLE-AND-HOLD	
AN OUTPUT CODE EITHER 15 OR 15.5 COUNTS	TRANSITION PT
FROM A MAJOR BIT COUNT	
A COMPARISON OF ACTUAL VOLTAGE AND A	TRANSITION WIDTH
TRANSITION COMPARED TO THE THEORETICAL VALUE	
ANALOG OR DIGITAL GROUND, NOT CONNECTED	GND
TO CHASSIS GROUND	
AMP-LOGIC CARD IN SLOT A-03 (SIGN)	
AMP-LOGIC CARD IN SLOT A-05 (SIGN)	
AMP-LOGIC CARD IN SLOT A-06 (AGG)	
AMP-LOGIC CARD IN SLOT A-07 (AGG)	
AMP-LOGIC CARD IN SLOT A-08 (AGG)	
AMP-LOGIC CARD IN SLOT A-09 (SIGN)	
AMP-LOGIC CARD IN SLOT A-10 (SIGN)	
AMP-LOGIC CARD IN SLOT A-11 (SIGN)	
AMP-LOGIC CARD IN SLOT A-12 (AGG)	
AMP-LOGIC CARD IN SLOT A-13 (AGG)	
AMP-LOGIC CARD IN SLOT A-14 (AGG)	
EXTERNAL PRECISION SOURCE	CALIBRATOR
DIFFERENCE IN OUTPUT LEVELS OF 8-H FOR THE	DIFF
SAMPLE AND HOLD TIMES	
OPERATION AND MAINTENANCE MANUAL FOR	MANUAL
RAIN 58855 SYSTEM	
GMM MULTIPLEXER (FET SWITCH ONLY)	RET-MUX
GND AMPLIFIER-MULTIPLEXER	RET-MUX
FREESTON PART NUMBER 52308 OR 52309 AS NOTED	OPERATION COVER

SYSTEM OPERATION & CONTROL

THE ADC-MUX SYSTEM HAS OFF-LINE CONTROLS WHICH MAY BE USED TO EASILY DETERMINE WHETHER IT IS WORKING PROPERLY. HOWEVER EVEN IN THE OFF-LINE MODE EXTERNAL CONNECTIONS FROM J2-52 TO J2-54 & J2-60 TO J2-80 ARE REQUIRED. THIS CONNECTS INT MUX CLOCK TO INT TADC, AND ZERO CONT TO GND, WHICH ALLOWS FRONT PANEL CONTROLS TO OPERATE IN ALL THEIR MODES. A SIGNAL SOURCE SHOULD BE CONNECTED TO AT LEAST ONE ANALOG INPUT. THE BEST STARTING POINT WOULD BE A FET INPUT CHANNEL (4 THRU 19) TO ELIMINATE OFFSET OR GAIN ERRORS THAT MAY BE PRESENT IN AMP-MUX CHANNELS. IT IS ALSO RECOMMENDED THAT ALL UNUSED ANALOG INPUTS BE GROUNDED.

PLACE ADC SWITCH TO NORM POSITION
MUX SWITCH TO CONTINUOUS RANDOM POSITION
FIRST MUX CHANNEL SWITCHES TO ADDRESS CH4.

THE ADC CONVERTER SHOULD NOW BE RUNNING ON ITS HI-SPEED INTERNAL CLOCK AND CONTINUOUSLY DIGITIZING CH4 AT THIS RATE. IF THE INPUT IS VARIED FROM -FS TO FS THE ADC OUTPUT AS INDICATED BY FRONT PANEL LEDS CAN BE OBSERVED. FOR A QUICK CHECK IT WILL ONLY BE NECESSARY TO MONITOR THE COUNTING SEQUENCE FOR PROPER OPERATION AS FOLLOWS:

(THE OUTPUT GOES FROM -FS(100000000000000) TO + FS(011111111111111) IN AN INCREASING MANNER AS THE INPUT IS INCREASED). IF THE ADC OUTPUT APPEARS CORRECT IT IS PROBABLY WORKING ALTHOUGH IT MAY STILL BE OUT OF CALIBRATION TOLERANCE. THE MUX ADDRESS INDICATORS SHOULD DISPLAY CH4.

TO CHECK CALIBRATION AN ACCURATE DC SOURCE IS REQUIRED. IT SHOULD BE VARIABLE FROM +/- FS. ON CH 4 THIS IS +/- 10.24V WITH A RESOLUTION OF .1MV. OTHER RANGES REQUIRE DIFFERENT FULL-SCALES TO VERIFY AMP-MUX CALIBRATION BUT THE +/- 10.24 VFS IS ADEQUATE TO CHECK THE ADC. A CHECK OF MAJOR BITS CAN BE MADE BY PUTTING IN VOLTAGES REQUIRED TO PRODUCE CODES SHOWN ON DATA SHEET IN TEST REPORT.

IT IS ALSO NECESSARY TO CHECK OTHER MODES OF OPERATION TO BE SURE ALL CONTROLS AND ALL OTHER ANALOG INPUT CHANNELS ARE WORKING. WITH ROTARY SWITCH STILL IN RANDOM USE FIRST CHANNEL MUX SWITCHES TO ADDRESS ALL OTHER CHANNELS (0 >>> 19) AND VERIFY A NEAR ZERO INDICATION ON THE ADC INDICATORS. IF EXPANSION CHASSIS IS CONNECTED ALSO VERIFY OUTPUT OF CH20 >>> CH 55 AND CH64 >>> CH103 INDICATE NEAR ZERO INPUTS. MUX INDICATORS SHOULD DISPLAY THE CHANNEL BEING ADDRESSED.

IN RANDOM MAN POSITION THE ADC SHOULD ADVANCE AND DIGITIZE THE CHANNEL ADDRESSED BY FIRST CH MUX SWITCHES EACH TIME THE MAN PB IS DERPRESSED.

SYSTEM OPERATION & CONTROLS

THE ADC-MUX SYSTEM HAS OFF-LINE CONTROLS WHICH MAY BE USED TO EASILY DETERMINE WHETHER IT IS WORKING PROPERLY. HOWEVER, SINCE THE OFF-LINE MODE EXTERNAL CONNECTIONS FROM J5-25 TO J5-24 & J5-25 TO J5-24 ARE REQUIRED, THIS CONNECTS INT MUX CLOCK TO INT TADC, AND ZERO CONT TO AND WHICH ALLOWS FRONT PANEL CONTROLS TO OPERATE IN ALL THEIR MODES. A SIGNAL SOURCE SHOULD BE CONNECTED TO AT LEAST ONE ANALOG INPUT. THE FIRST STARTING POINT WOULD BE A FET INPUT CHANNEL (A THRU 19) TO ELIMINATE OFFSET OR GAIN ERRORS THAT MAY BE PRESENT IN ANY-MUX CHANNELS. IT IS ALSO RECOMMENDED THAT ALL DELTA ANALOG INPUTS BE

PLEASE ADC SWITCH TO NORM POSITION
MUX SWITCH TO CONTINUOUS RANDOM POSITION
FIRST MUX CHANNEL SWITCHES TO ADDRESS CH4

THE ADC CONVERTER SHOULD NOW BE RUNNING ON ITS HI-SPEED INTERNAL CLOCK AND CONTINUOUSLY DIGITIZING CH4 AT THIS RATE. IF THE INPUT IS VARIOUS FROM 45 TO 55 THE ADC OUTPUT AS INDICATED BY FRONT PANEL LEDS CAN BE OBSERVED. FOR A QUICK CHECK IT WILL ONLY BE NECESSARY TO MONITOR THE COUNTING SEQUENCE FOR PROPER OPERATION AS FOLLOWS:

(THE OUTPUT GOES FROM -F8(10000000000) TO +F8(0000000000)) IN AN INCREASING MANNER AS THE INPUT IS INCREASED. IF THE ADC OUTPUT ERRORS CORRECT IT IS PROBABLY WORKING ALTHOUGH IT MAY STILL BE OUT OF CALIBRATION TOLERANCE. THE MUX ADDRESS INDICATORS SHOULD DISPLAY

TO CHECK CALIBRATION AN ACCURATE DC SOURCE IS REQUIRED. IT SHOULD BE VARIABLE FROM +V- FS. ON CH 4 THIS IS +/- 10 24V WITH A RESOLUTION OF 1MV. OTHER RANGES REQUIRE DIFFERENT FULL-SCALES TO VERIFY AND-MUL CALIBRATION BUT THE +/- 10 24V IS ADEQUATE TO CHECK THE ADC. A CHECK ON MAJOR STS CAN BE MADE BY PUTTING IN VOLTAGE ADJUSTED TO PRODUCE CODES SHOWN ON DATA SHEET IN TEST REPORT.

IF THE SYSTEM IS NOT WORKING PROPERLY, IT IS OF OPERATION TO BE SHOWN. ALL CHANNELS (0-15) AND VERIFY A NEAR ZERO INDICATION ON THE ADC. THE FIRST STARTING POINT WOULD BE A FET INPUT CHANNEL (A THRU 19) TO ELIMINATE OFFSET OR GAIN ERRORS THAT MAY BE PRESENT IN ANY-MUX CHANNELS. IT IS ALSO RECOMMENDED THAT ALL DELTA ANALOG INPUTS BE

PLEASE ADC SWITCH TO NORM POSITION
MUX SWITCH TO CONTINUOUS RANDOM POSITION
FIRST MUX CHANNEL SWITCHES TO ADDRESS CH4

SEQUENTIAL OPERATION SHOULD ALSO BE VERIFIED. THIS CAN BE DONE BY FIRST USING SEQ MAN POSITION AND SETTING UP FIRST AND LAST CHANNEL MUX ADDRESSES WITH CORRESPONDING FP SWITCHES. BE SURE THAT LAST CHANNEL ADDRESS IS GREATER THAN THE FIRST CHANNEL ADDRESS. IF NOT CORRECT OPERATION WILL NOT OCCUR. WITH FIRST AND LAST ADDRESSES EQUAL THE ADC WILL DIGITIZE THIS CHANNEL EACH TIME THE MAN PB IS DEPRESSED. WITH THE LAST CHANNEL GREATER THAN THE FIRST CHANNEL THE MUX WILL SEQUENCE FROM FIRST TO LAST CHANNEL, ADVANCING ONE CHANNEL EACH TIME THE MAN PB IS DEPRESSED. PROPER SEQUENTIAL OPERATION WILL BEGIN WHEN THE CHANNEL ADDRESSED IS EQUAL OR GREATER THAN THE SELECTED FIRST CHANNEL AND LESS THAN OR EQUAL TO THE SELECTED LAST CHANNEL.

EXAMPLE:

FIRST CHANNEL ADDRESSED = 4

LAST CHANNEL ADDRESSED = 9

CHANNEL PREVIOUSLY ADDRESSED = 14

THE COUNTER WILL ADVANCE FROM CH14 TO MAXIMUM COUNT(CH255) BEFORE RETURNING TO CH0 AND THEN COUNTING UP AGAIN. WHEN IT REACHES CH4 THE PROPER SEQUENCE WILL BEGIN. IN THE CONTINUOUS SEQUENTIAL MODE THIS WOULD NOT BE NOTICED BUT IN THE MANUAL MODE IT MAY APPEAR AS A PROBLEM UNLESS THE CONDITION IS RECOGNIZED.

IN THE CONTINUOUS SEQUENTIAL MODE IT IS NOT POSSIBLE TO OBSERVE EVERY CHANNEL IN ORDER BUT A CHECK OF MUX ADDRESS TEST POINTS ON THE MUX CARDS WILL SHOW IF THE CORRECT SEQUENCE IS BEING RUN. BY SYNCING ON COIN (TRUE FOR LAST CH) THE MUX ADDRESS POSITION CAN BE SEEN TO ADVANCE ONE POSITION FOR EACH SUCCESSIVE CHANNEL.

THE ADC ALSO HAS AN INTERNAL CLOCK OF APPROXIMATELY 10HZ AND A MANUAL PB WHICH MAY BE USED IN NON-MULTIPLEXING MODES. THESE ARE NOT SYNCHRONIZED WITH THE INTERNAL MUX CLOCK. THESE MODES CAN BE CHECKED FOR PROPER OPERATION BUT ARE NOT RECOMMENDED FOR CALIBRATION.

SINCE IT IS RELATIVELY EASY TO VERIFY ALL INTERNAL OPERATING MODES AND LITTLE EXTERNAL EQUIPMENT IS REQUIRED THIS SHOULD BE DONE BEFORE CHECKING EXTERNAL MODES.

SEQUENTIAL OPERATION SHOULD ALSO BE VERIFIED. THIS CAN BE DONE BY FIRST USING 320 MAN POSITION AND SETTING UP FIRST AND LAST CHANNEL MUX ADDRESS WITH CORRESPONDING PR SWITCHES. BE SURE THAT LAST CHANNEL ADDRESS IS GREATER THAN THE FIRST CHANNEL ADDRESS. IF NOT CORRECT OPERATION WILL NOT OCCUR. WITH FIRST AND LAST ADDRESSES EQUAL THE ADD WILL DIVIDE THIS CHANNEL EACH TIME THE MAN PR IS DEPRESSED. WITH THE LAST CHANNEL GREATER THAN THE FIRST CHANNEL THE MUX WILL SEQUENCE FROM FIRST TO LAST CHANNEL, ADVANCING ONE CHANNEL EACH TIME THE MAN PR IS DEPRESSED. PROPER SEQUENTIAL OPERATION WILL BEGIN WHEN THE CHANNEL ADDRESS IS EQUAL OR GREATER THAN THE SELECTED FIRST CHANNEL AND LESS THAN OR EQUAL TO THE SELECTED LAST CHANNEL.

EXAMPLE:

FIRST CHANNEL ADDRESS = 4
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THE COUNTER WILL ADVANCE FROM CH14 TO MAXIMUM COUNT (CH255) BEFORE RETURNING TO CH0 AND THEN COUNTING UP AGAIN. WHEN IT REACHES CH0 THE PROPER SEQUENCE WILL BEGIN. IN THE CONTINUOUS SEQUENTIAL MODE THIS WOULD NOT BE NOTICED BUT IN THE MANUAL MODE IT MAY APPEAR AS A PROBLEM. UNLESS THE CONDITION IS RECOGNIZED.

IN THE CONTINUOUS SEQUENTIAL MODE IT IS NOT POSSIBLE TO REVERSE ENTRY CARDS WILL SHOW IF THE CORRECT SEQUENCE IS BEING RUN. BY SYNCING ON CH0 (TRUE FOR LAST CH) THE MUX ADDRESS POSITION CAN BE GIVEN TO ADVANCE ONE POSITION FOR EACH SUCCESSIVE CHANNEL.

THE ADD ALSO HAS AN INTERNAL CLOCK OF APPROXIMATELY 10HZ AND A MANUAL PR WHICH MAY BE USED IN NON-MULTIPLEXING MODES. THESE ARE NOT SYNCED WITH THE INTERNAL MUX CLOCK. THESE MODES CAN BE CHECKED FOR PROPER OPERATION BUT ARE NOT RECOMMENDED FOR CALIBRATION.

SINCE IT IS RELATIVELY EASY TO VERIFY ALL INTERNAL OPERATING MODES AND LITTLE EXTERNAL EQUIPMENT IS REQUIRED THIS SHOULD BE DONE BEFORE CHECKING EXTERNAL MODES.

EXTERNAL CONTROLS & TIMING

FIGURE TMX-1 SHOWS THE INPUT SIGNALS WHICH MUST BE CONTROLLED BY EXTERNAL DEVICES IF THEY ARE TO BE USED. ALL SIGNALS MAY NOT BE NEEDED FOR EACH TEST STATION BUT PROPER LEVELS MUST BE MAINTAINED IF NOT USED. MANUAL SWITCHES SHOWN COULD BE REPLACED BY TTL OUTPUT GATES CONTROLLED BY SOME PROGRAMMABLE DEVICE.

WITH THESE SWITCHES, ALL EXTERNAL CONTROLS MAY BE CHECKED FOR PROPER OPERATION. USING AN EXTERNAL CLOCK, THE SYSTEM MAY BE OPERATED AT ANY SPEED UP TO THE MAXIMUM CONVERSION RATE. IF THE SYSTEM IS CLOCKED AT A RATE GREATER THAN THE MAXIMUM SPECIFIED IN THE TEST REPORT, THE OUTPUT DATA WILL BE INVALID.

MAXIMUM CONVERSION RATE IS DEPENDENT UPON THE NUMBER OF CHANNELS BEING MULTIPLEXED AND IS GIVEN IN THE APPLICABLE SPECIFICATION(S). THIS INFORMATION IS ALSO GIVEN ON THE TEST REPORT SUPPLIED WITH EACH UNIT. FOR HI-SPEED A/D SYSTEMS SUCH AS THE 58700 SYSTEM, TIMING IS VERY CRITICAL AND SHOULD NOT BE ADJUSTED WITHOUT A THOROUGH KNOWLEDGE OF THE UNIT AND THE GMAD1 ADC CHARACTERISTICS. IF, AS THE RESULT OF A TIMING RELATED MALFUNCTION, THE TIMING CARD MUST BE REPAIRED AND IT IS NECESSARY TO REPLACE A COMPONENT(S) OR TO RE-ADJUST THE TIMING CARD THE ORIGINAL TEST REPORT SHOULD BE USED AS A GUIDE TO SET THE DELAYS.

BY TRIGGERING A SCOPE ON THE EXT CLOCK INPUT THE VARIOUS DELAYS CAN BE OBSERVED AND IF NECESSARY ADJUSTED TO VALUES SHOWN ON ORIGINAL TIMING DIAGRAM. IT IS A GOOD PRACTICE TO MAKE A TIMING DIAGRAM ON THE UNIT BEFORE MAKING ANY ADJUSTMENTS. THEN A RECORD OF ACTUAL TIMING EXISTS. TYPICALLY HI-SPEED SYSTEMS HAVE SIMILAR BUT NOT IDENTICAL TIMING. EXACT TIMING IS FACTORY SET DURING FINAL TEST TO WHERE THE PARTICULAR UNIT PERFORMS BEST.

A COPY OF THE TEST REPORT FROM UNIT S/N RAA -1000 IS INCLUDED. AT THE MAXIMUM EXTERNAL CLOCK FREQUENCY OF APPROXIMATELY 286 KHZ (3.5 MICROSECOND CONVERSION RATE) IT CAN BE NOTED THAT EOC(INDICATING CONVERSION IS COMPLETE) DOES NOT APPEAR UNTIL AFTER THE SECOND INPUT CLOCK. THIS IS DEFINED AS "OVERLAPPED TIMING" AND IS TYPICAL OF GMAD1 ADC SYSTEMS. FOR A SINGLE CONVERSION THE TIME REQUIRED IS APPROXIMATELY 4 MICROSECONDS BUT THE 3.5 MICROSECOND RATE CAN BE MAINTAINED AFTER THIS FIRST CONVERSION.

EXTERNAL CONTROLS & TIMING

FIGURE 1-1 shows the input signals which must be controlled by external devices if they are to be used. All signals may not be needed for each test station but proper levels must be maintained if not used. Manual switches shown could be replaced by TTL output gates controlled by some

with these switches. All external controls may be checked for proper operation. Using an external clock, the system may be operated at any speed up to the maximum conversion rate. If the system is clocked at a rate greater than the maximum specified in the test report, the output data will be invalid.

Maximum conversion rate is dependent upon the number of channels being multiplexed and is given in the applicable specification(s). This information is also given on the test report supplied with each unit. For hi-speed A/D systems such as the 5800 system, timing is very critical and should not be adjusted without a thorough knowledge of the unit and the A/D characteristics. If, as the result of a timing related malfunction, the timing card must be repaired and it is necessary to replace a component(s) or to re-adjust the timing card, the test report should be used as a guide to set the delays.

By triggering a scope on the EXT CLOCK input the various delays can be observed and, if necessary, adjusted to values shown on original timing diagram. It is a good practice to make a timing diagram on the unit before making any adjustments. Then a record of actual timing is obtained. Typically, hi-speed systems have similar but not identical timing. Exact timing is factory set during final test to where the particular unit performs best.

A copy of the test report from unit 57N RAA-1000 is included. At this maximum external clock frequency of approximately 285 kHz (3.5 microseconds conversion rate) it can be noted that the second input (conversion is complete) does not appear until after the second input clock. This is defined as "overlapped timing" and is typical of A/D systems. For a single conversion the time required is approximately 4 microseconds but the 3.5 microsecond rate can be maintained after this first conversion.

***** ADC THEORY OF OPERATION *****

THE ADC BY ITSELF OPERATES AS A +/- 10 VOLT FULL-SCALE DEVICE. SCALING IF REQUIRED IS DONE ON THE SAMPLE-AND-HOLD. IN ADDITION TO THE ANALOG INPUT

THE ADC ALSO REQUIRES A STABLE + 10 VOLT REFERENCE AND TWO GATING SIGNALS. THE FIRST SIGNAL(GATE1), UP-DATES THE 11 MOST SIGNIFICANT BITS AND THE SECOND SIGNAL(GATE2), UP-DATES THE 4 LEAST SIGNIFICANT BITS.

THE ADC IS MADE UP OF A SERIES OF AMP-LOGIC CARDS (1 PER BIT FOR THE 11 MOST SIGNIFICANT BITS), AND A PAIR OF CARDS(4 BIT AMP AND 4 BIT LOGIC) FOR THE LAST FOUR BITS. BLOCK DIAGRAM TMX-23 SHOWS HOW BOARDS ARE CONNECTED IN SERIES WITH ANALOG OUTPUT OF THE FIRST AMP-LOGIC CARD(MSB = SIGN+) CONNECTED TO THE ANALOG INPUT OF THE NEXT AMP-LOGIC CARD(DB8192). A DIGITAL SIGNAL IS ALSO PASSED ON FROM ONE CARD TO THE NEXT. THE LOGIC OUTPUT FOR A GIVEN CARD IS DEPENDENT UPON THE DIGITAL INPUT TO THE CARD AND THE POLARITY OF THE ANALOG INPUT TO THAT CARD.

THE DIGITAL INPUT TO THE FIRST CARD (SIGN) NORMALLY ONE LOGIC INPUT OPEN AND THE COMPLEMENT STRAPPED TO GND BUT THE 58700 ADC HAS A UNIQUE " ZERO CROSSING CONTROL " FEATURE. THE ZERO CONT INPUT SIGNAL AND ITS COMPLEMENT SUPPLY THE LOGIC INPUTS TO THE FIRST CARD. IF THIS CONTROL IS NOT USED THIS INPUT MUST BE KEPT AT GROUND. IF THIS SIGNAL GOES TRUE THE ADC OUTPUT IS ONLY USED TO INDICATE POLARITY OF THE INPUT. AN OPEN INPUT WILL CAUSE UNPREDICTABLE OPERATION AND SINCE A TTL OPEN INPUT ACTS MORE LIKE A TRUE SIGNAL THE ADC WILL BE IN THE ZERO CROSSING MODE BUT THE OUTPUT WILL NOT BE CERTAIN.

THE TRANSFER FUNCTION FOR THE ANALOG SIGNAL THRU THE FIRST 11 MOST SIGNIFICANT BIT CARDS IS $V_{OUT} = 2 \cdot |V_{IN}| - 10$. USING THIS FORMULA THE THEORETICAL ANALOG OUTPUT OF EACH CARD IN AN ADC CAN BE CALCULATED. AS INDICATED ON BLOCK DIAGRAM TMX-23 THE LAST 4 BITS ARE ACTUALLY MECHANIZED WITH DIFFERENT HARDWARE BUT THE CALCULATION IS STILL VALID. THE KEY TO THE OPERATION IS THE "POLARITY" --INTO-- EACH CARD WHICH , EXCEPT FOR THE FIRST CARD, DEPENDS UPON THE PREVIOUS CARD(S).

***** ADC THEORY OF OPERATION *****

THE ADC BY ITSELF OPERATES AS A +/- 10 VOLT FULL-SCALE DEVICE. SCALING IS REQUIRED TO THE ANALOG INPUT. IN ADDITION TO THE ANALOG INPUT.

THE ADC ALSO REQUIRES A STABLE +/- 10 VOLT REFERENCE AND TWO GATING SIGNALS. THE FIRST SIGNAL(GATE1), UP-DATES THE 11 MOST SIGNIFICANT BITS AND THE SECOND SIGNAL(GATE2), UP-DATES THE 4 LEAST SIGNIFICANT BITS.

THE ADC IS MADE UP OF A SERIES OF AMP-LOGIC CARDS (1 PER BIT FOR THE 11 MOST SIGNIFICANT BITS), AND A PAIR OF CARDS (4 BIT AMP AND 4 BIT LOGIC) FOR THE LAST FOUR BITS. BLOCK DIAGRAM TMX-23 SHOWS HOW BOARDS ARE CONNECTED IN SERIES WITH ANALOG OUTPUT OF THE FIRST AMP-LOGIC CARD(NEED A SIGN-) CONNECTED TO THE ANALOG INPUT OF THE NEXT AMP-LOGIC CARD(NEEDS). A DIGITAL SIGNAL IS ALSO PASSED ON FROM ONE CARD TO THE NEXT. THE LOGIC OUTPUT FOR A GIVEN CARD IS DEPENDENT UPON THE DIGITAL INPUT TO THE CARD AND THE POLARITY OF THE ANALOG INPUT TO THAT CARD.

THE DIGITAL INPUT TO THE FIRST CARD (SIGN) NORMALLY ONE LOGIC INPUT OPEN AND THE COMPLEMENT STRAPPED TO GND BUT THE 8200 ADC HAS A UNIQUE "ZERO CROSSING CONTROL" FEATURE. THE ZERO CONT INPUT SIGNAL AND ITS COMPLEMENT SUPPLY THE LOGIC INPUTS TO THE FIRST CARD. IF THIS CONTROL IS NOT USED THIS INPUT MUST BE KEPT AT GROUND. IF THIS SIGNAL GOES FROM THE ADC OUTPUT IS ONLY USED TO INDICATE POLARITY OF THE INPUT. AN INPUT THAT WILL CAUSE UNPREDICTABLE OPERATION AND SINCE A TRUE SIGNAL INPUT ACTS MORE LIKE A TRUE SIGNAL THE ADC WILL BE IN THE ZERO CROSSING MODE BUT THE OUTPUT WILL NOT BE CERTAIN.

THE TRANSFER FUNCTION FOR THE ANALOG SIGNAL THRU THE FIRST 11 MOST SIGNIFICANT BIT CARDS IS $V_{OUT} = 2^N \cdot V_{IN} - 10$. USING THIS FORMULA THE THEORETICAL ANALOG OUTPUT OF EACH CARD IN AN ADC CAN BE CALCULATED. AS INDICATED ON BLOCK DIAGRAM TMX-23 THE LAST 4 BITS ARE ACTUALLY DETERMINED WITH DIFFERENT HARDWARE BUT THE CALCULATION IS STILL VALID. THE KEY TO THE OPERATION IS THE "POLARITY" ---INTC--- EACH CARD WHICH EXCEPT FOR THE FIRST CARD, DEPENDS UPON THE PREVIOUS CARD'S

THE DIGITAL OUTPUT OR CARRY OF EACH CARD DEPENDS UPON THE POLARITY OF THE ANALOG "INPUT" AND THE STATE OF THE DIGITAL INPUT (WHICH EXCEPT FOR THE FIRST CARD IS THE CARRY OUT FROM THE PREVIOUS CARD. THE TRUTH TABLE IS: (REFERENCE BLOCK DIAGRAM TMX-23).

ANALOG INPUT POLARITY	LOGIC INPUT	LOGIC OUTPUT
POSITIVE	TRUE	1
NEGATIVE	FALSE	1
POSITIVE	FALSE	0
NEGATIVE	TRUE	0

THE REFERENCED BLOCK DIAGRAM IS MADE BY COMPUTER PROGRAM WITH ANY RANDOM VOLTAGE FROM +/- FULL-SCALE USED AS AN INPUT. THE VOLTAGE AT THE ADC INPUT HAS BEEN SCALED BY THE SAMPLE-AND -HOLD FOR THE REQUIRED +/- 10 VOLTS USED BY THE ADC.

LOGIC OUTPUTS OF THE ADC CARDS CHANGE ONLY AFTER THE CORRESPONDING GATE SIGNALS ARE RECEIVED. AN EOC (END-OF-CONVERSION) PULSE IS GENERATED BY THE ADC TIMING CARD APPROXIMATELY 400 NANoseconds AFTER THE LEADING EDGE OF GATE1. THIS DELAY ALLOWS DIGITAL OUTPUT LINES TIME TO SETTLE BEFORE SIGNALLING THAT CONVERSION IS COMPLETE. DATA REMAINS STABLE UNTIL THE NEXT GATE1 PULSE. THE TIME DEPENDS UPON THE EXTERNAL TRIGGER RATE OR UPON THE INTERNAL MUX CLOCK. IF RUNNING FROM AN EXTERNAL TRIGGER SOURCE THE DATA MUST BE TAKEN BEFORE THE NEXT GATE1 PULSE OR IT IS LOST. THE BUSY* SIGNAL CORRESPONDS TO A DATA VALID SIGNAL.

TABLE 12. (REFERENCE BLOCK DIAGRAM TMX-23).
 THE FIRST CARD IS THE CARRY OUT FROM THE PREVIOUS CARD. THE TRUTH
 THE ANALOG "INPUT" AND THE STATE OF THE DIGITAL INPUT WHICH EXCEPT FOR
 THE DIGITAL OUTPUT OR CARRY OF EACH CARD DEPENDS UPON THE POLARITY OF

ANALOG INPUT POLARITY	LOGIC INPUT	LOGIC OUTPUT
POSITIVE	TRUE	1
NEGATIVE	FALSE	1
POSITIVE	FALSE	0
NEGATIVE	TRUE	0

THE REFERENCED BLOCK DIAGRAM IS MADE BY COMPUTER PROGRAM WITH ANY
 RANDOM VOLTAGE FROM ± 1 FULL-SCALE USED AS AN INPUT. THE VOLTAGE AT
 THE ADC INPUT HAS BEEN SCALED BY THE SAMPLE-AND-HOLD FOR THE REQUIRED
 ± 1 10 VOLTS USED BY THE ADC.

LOGIC OUTPUTS OF THE ADC CARDS CHANGE ONLY AFTER THE CORRESPONDING GATE
 SIGNALS ARE RECEIVED. AN EOC (END-OF-CONVERSION) PULSE IS GENERATED BY
 THE ADC TIMING CARD APPROXIMATELY 400 NANOSECONDS AFTER THE LEADING
 EDGE OF GATE1. THIS DELAY ALLOWS DIGITAL OUTPUT LINES TIME TO SETTLE
 BEFORE SIGNALING THAT CONVERSION IS COMPLETE. DATA REMAINS STABLE
 UNTIL THE NEXT GATE1 PULSE. THE TIME DEPENDS UPON THE EXTERNAL TRIGGER
 RATE OR UPON THE INTERNAL MUX CLOCK. IF RUNNING FROM AN EXTERNAL
 TRIGGER SOURCE THE DATA MUST BE TAKEN BEFORE THE NEXT GATE1 PULSE OR IT
 IS LOST. THE BUSY SIGNAL CORRESPONDS TO A DATA VALID SIGNAL.

***** ADC TROUBLE-SHOOTING *****

BEFORE ANY TROUBLE-SHOOTING IN THE ADC CAN BE ATTEMPTED IT IS NECESSARY TO KNOW WHAT TO EXPECT AT THE ADC OUTPUT FOR A GIVEN INPUT. SINCE THE ADC OUTPUT IS A BINARY NUMBER PROPORTIONAL TO THE ANALOG INPUT IT IS NECESSARY TO RECOGNIZE THE PATTERN OF THE BINARY DISPLAY. FIG TMX-19 SHOWS TYPICAL OUTPUTS FOR A TWO'S COMPLEMENT ADC WITH A SELECTION OF INPUTS SIMILAR TO VOLTAGES FOUND ON THE DATA SHEET OF THE TEST REPORT. THE 1'S CORRESPOND "ON" INDICATORS AND ZERO'S CORRESPOND TO "OFF" INDICATORS. THE ADC HAS BOTH DATA AND COMPLEMENTS BROUGHT THE REAR CONNECTOR. THE SIGN+ IS A ONE WHEN THE POLARITY IS POSITIVE. THEREFORE IT IS NECESSARY TO USE THE SIGN- FOR A TRUE TWO'S COMPLEMENT OUTPUT. WHEN PROPERLY OPERATING THE SIGN+ IS ON AND THE FP INDICATORS INCREASE FROM ALL OFF (0V INPUT) TO ALL ON (+FS INPUT) IN A BINARY SEQUENCE AS A POSITIVE ANALOG INPUT IS APPLIED. FOR A NEGATIVE INPUT THE SIGN- IS ON AND THE INDICATORS GO FROM ALL ON (- ONE COUNT) TO ALL OFF (-FS INPUT) IN A BINARY SEQUENCE AS THE ANALOG IS VARIED FROM NEAR 0V TO -FS. FOR A QUICK TEST A PRECISE SOURCE IS NOT REQUIRED. A LOW FREQUENCY TRIANGULAR WAVEFORM IS USEFUL BECAUSE IT ALLOWS OBSERVER TO CONCENTRATE ON THE DISPLAY INSTEAD OF ADJUSTING THE INPUT SOURCE.

BY SLOWLY VARYING THE ANALOG INPUT AND OBSERVING THE FP INDICATORS IT IS POSSIBLE TO RAPIDLY SEE WHETHER THE ADC IS OPERATING CORRECTLY. IF THE OUTPUT DOES NOT COUNT PROPERLY BUT REVERSES WHEN REACHING A CERTAIN BIT THERE IS A PROBLEM, PROBABLY ASSOCIATED WITH OF THE AMP-LOGIC CARD CORRESPONDING TO THIS BIT. THE PROBLEM MAY BE CAUSED BY A DIGITAL OR ANALOG FAILURE OR MAY BE THE RESULT OF A FAILURE OF THE CARD BEFORE OR AFTER THE SUSPECTED CARD.

THE ANALOG OUTPUT MAY BE EASILY VERIFIED BY MONITORING THE A2 TEST POINT ON THE AMP-LOGIC CARD WHILE APPLYING KNOWN INPUTS. SINCE ALL AMP-LOGIC CARDS HAVE THE SAME TRANSFER FUNCTION $V_{OUT} = 2 \cdot (V_{IN}) - 10$ THE FOLLOWING QUICK CHECK IS APPLICABLE TO ALL AMP-LOGIC CARDS.

VIN(APPLIED)	VOUT(MEASURED)
0V	-10V*
- 5V	0V
+ 5V	0V
-10V	+10V
+10V	+10V

* IF THE -10V OFFSET IS NOT CORRECT FIRST CHECK THE +10V REF SUPPLY WHICH IS THE SOURCE OF THIS OFFSET.

IF THE VOLTAGES ARE CORRECT THE ANALOG PORTION IS OK AND THE PROBLEM IS DIGITAL.

DIGITAL PROBLEMS ARE MOST EASILY FOUND BY FIRST SUBSTITUTING ANOTHER AMP-LOGIC CARD INTO THE SLOT BELIEVED TO HAVE THE PROBLEM TO DETERMINE WHETHER THIS IS REALLY THE PROBLEM CARD. ALL AMP-LOGIC CARDS ARE PIN COMPATIBLE AND HAVE THE SAME CHARACTERISTICS SO ANY CARD MAY BE USED. HOWEVER THE AMP-LOGIC LOGIC "A" CARDS CANNOT SUPPLY THE REQUIRED DRIVE CURRENT FOR THE "B" OR "C" CARDS SO THE BEST CHOICE IS A "B" CARD. THIS MAY BE USED IN ANY AMP-LOGIC SLOT. NOTE: AS STATED, THE PROBLEM CARD MAY BE THE ONE BEFORE OR AFTER THE ONE THAT CORRESPONDS TO THE BIT THAT HAS THE PROBLEM. THE PREVIOUS CARD MAY NOT BE ABLE TO DRIVE THE CARD SUSPECTED OR THE FOLLOWING CARD MAY BE LOADING THE OUTPUT SIGNAL TO A POINT WHERE IT WILL NOT FUNCTION. WHEN THE PROBLEM CARD IS LOCATED STANDARD DIGITAL TROUBLE-SHOOTING TECHNIQUES MAY BE USED TO FIND THE PARTICULAR MALFUNCTION. THE PRIMARY IMPORTANCE IS TO LOCATE THE DEFECTIVE CARD.

TROUBLE-SHOOTING MUST BE DONE WITH THE TOP COVER REMOVED SO ANALOG OUTPUTS MAY DRIFT AROUND AND PRECISE ANALOG MEASUREMENTS ARE NOT VALID. A SPECIAL BIT BOARD SUBSTITUTION CARD, PRESTON P/N 52330 IS REQUIRED TO CONNECT ANALOG INPUT SIGNALS INTO THE AMP-LOGIC CARDS. FOR TROUBLE-SHOOTING THE DC CALIBRATOR REMOTE SENSE LINES ARE NOT NECESSARY BUT FOR ADC CALIBRATION THEY ARE ESSENTIAL BECAUSE AMP-LOGIC CARDS HAVE RELATIVELY LOW INPUT IMPEDANCE (2 TO 4 K OHMS).

A PREFERRED TROUBLE-SHOOTING AID IS A COMPLETE SET OF ONE OF EACH TYPE PLUG-IN CARD IN THE SYSTEM. PROBLEM CARDS CAN MOST RAPIDLY BE LOCATED BY SUBSTITUTION. THIS METHOD STILL HAS LIMITATIONS IN THAT SUBSTITUTION MAY BE USED FOR FINDING A PROBLEM BUT IN MANY CASES THE ORIGINAL CARD MUST BE REPLACED WHEN IT IS REPAIRED. IT CANNOT BE OVER-EMPHASIZED THAT THE ADC-MUX SYSTEM IS CALIBRATED AS A "SYSTEM" AND THAT ONE SECTION MAY BE OUT OF ITS INDIVIDUAL TOLERANCE TO COMPENSATE FOR ANOTHER SECTION. THIS IS NORMAL. THEREFORE A CALIBRATED AMP-LOGIC CARD MAY NOT APPEAR CALIBRATED IN A GIVEN SLOT. IT IS FURTHER POSSIBLE THAT, IF THIS IS THE CASE, MAKING ADJUSTMENTS TO THE CARD WITHOUT USING THE PROPER SEQUENCE MAY MAKE IT APPEAR EVEN WORSE. THE BEST PRACTICE IS TO MAKE AN APPROXIMATE ANALOG CHECK AND IF OK, SUBSTITUTE CARDS TO FIND DIGITAL PROBLEM.

DIGITAL PROBLEMS ARE MOST EASILY FOUND BY FIRST SUBSTITUTING ANOTHER AMP-LOGIC CARD INTO THE SLOT BELIEVED TO HAVE THE PROBLEM TO DETERMINE WHETHER THIS IS REALLY THE PROBLEM CARD. ALL AMP-LOGIC CARDS ARE PIN IDENTICAL AND HAVE THE SAME CHARACTERISTICS SO ANY CARD MAY BE USED. HOWEVER THE AMP-LOGIC LOGIC "A" CARDS CANNOT SUPPLY THE REQUIRED DRIVE CURRENT FOR THE "B" OR "C" CARDS SO THE BEST CHOICE IS A "E" CARD. THIS MAY BE USED IN ANY AMP-LOGIC SLOT. NOTE: AS STATED, THE PROBLEM CARD MAY BE THE ONE BEFORE OR AFTER THE ONE THAT CORRESPONDS TO THE BIT THAT HAS THE PROBLEM. THE PREVIOUS CARD MAY NOT BE ABLE TO DRIVE THE CARD SUSPECTED OR THE FOLLOWING CARD MAY BE LOADING THE OUTPUT SIGNAL TO A POINT WHERE IT WILL NOT FUNCTION. WHEN THE PROBLEM CARD IS LOCATED STANDARD DIGITAL TROUBLE-SHOOTING TECHNIQUES MAY BE USED TO FIND THE PARTICULAR MALFUNCTION. THE PRIMARY IMPORTANCE IS TO LOCATE THE DEFECTIVE CARD.

TROUBLE-SHOOTING MUST BE DONE WITH THE TOP COVER REMOVED SO ANALOG OUTPUTS MAY DRIFT AROUND AND PRECISE ANALOG MEASUREMENTS ARE NOT VALID. A SPECIAL BIT BOARD SUBSTITUTION CARD, PRECISION PIN 55500 IS REQUIRED TO CONNECT ANALOG INPUT SIGNALS INTO THE AMP-LOGIC CARDS. FOR TROUBLE-SHOOTING THE DC CALIBRATOR REMOTE SENSE LINES ARE NOT NECESSARY BUT FOR ADC CALIBRATION THE ARE ESSENTIAL BECAUSE AMP-LOGIC CARDS HAVE RELATIVELY LOW INPUT IMPEDANCE (2 TO 4 K OHMS).

A PREFERRED TROUBLE-SHOOTING AID IS A COMPLETE SET OF ONE OF EACH TYPE PLUG-IN CARD IN THE SYSTEM. PROBLEM CARDS CAN MOST RAPIDLY BE LOCATED BY SUBSTITUTION. THIS METHOD STILL HAS LIMITATIONS IN THAT SUBSTITUTION MAY BE USED FOR FINDING A PROBLEM BUT IN MANY CASES THE ORIGINAL CARD MUST BE REPLACED WHEN IT IS REPAIRED. IT CANNOT BE OVER-EMPHASIZED THAT THE ADC-MUX SYSTEM IS CALIBRATED AS A "SYSTEM" AND THAT ONE SECTION MAY BE OUT OF ITS INDIVIDUAL TOLERANCE TO COMPENSATE FOR ANOTHER SECTION. THIS IS NORMAL. THEREFORE A CALIBRATED AMP-LOGIC CARD MAY NOT APPEAR CALIBRATED IN A GIVEN SLOT. IT IS FURTHER POSSIBLE THAT, IF THIS IS THE CASE, MAKING ADJUSTMENTS TO THE CARD WITHOUT USING THE PROPER SEQUENCE MAY MAKE IT APPEAR EVEN WORSE. THE BEST PRACTICE IS TO MAKE AN APPROXIMATE ANALOG CHECK AND IF OK, SUBSTITUTE CARDS TO FIND DIGITAL PROBLEM.

BASIC OPERATIONAL AMPLIFIER REF. (FIGURE TMX-2)

THIS FIGURE SHOWS THE BASIC STRUCTURE OF OP-AMPS USED THROUGHOUT THIS SYSTEM. SOME CIRCUITS HAVE MODIFICATIONS WHICH INCLUDE MORE COMPONENTS, BUT THE BASIC CIRCUIT STILL HAS THE SAME OPERATION.

OPERATION:

THE FOLLOWING ASSUMPTIONS ARE MADE:

- 1 CIRCUIT ADJUSTED FOR $V_{OUT} = 0V$ WHEN $V_{IN} = 0V$. (ADJUSTMENT CIRCUIT NOT SHOWN).
- 2 Q_{1A} AND Q_{1B} ARE MATCHED WITH CLOSE V_{SG} @ BIAS POINT.
- 3 V_{SG} APPROXIMATELY $= +1V$.
- 4 SINCE $Q_{1B} = 0V$; $Q_{1A} = 0V$.
- 5 $I_{D1} = I_{D2}$ (FETS ARE MATCHED PAIR)
- 6 Q_{2A} & Q_{2B} ARE MATCHED PAIR.
- 7 SINCE $V_{BA} = V_{BB}$ ----- $I_{CA} = I_{CB}$ MAKING $V_{OUT} = 0V$.

IF V_{OUT} STARTS TO GO POSITIVE, THIS (+) VOLTAGE IS FED BACK TO Q_{1A} GATE THRU R_F . THIS RESULTS IN A GREATER VOLTAGE DROP ACROSS R_{D1} THAN R_{D2} MAKING THE DRAIN VOLTAGE OF Q_{1A} (ALSO Q_{2A} BASE VOLTAGE) MORE NEGATIVE THAN THE DRAIN VOLTAGE OF Q_{1B} (ALSO Q_{2B} BASE VOLTAGE). THIS BIAS CONDITION CAUSES Q_3 TO CONDUCT MORE AND Q_5 TO CONDUCT LESS. Q_3 COLLECTOR GOES MORE NEGATIVE MAKING EMITTER FOLLOWER, Q_4 EMITTER MORE NEGATIVE. THIS NEGATIVE GOING OUTPUT IS FED BACK THRU R_F TO THE GATE OF Q_{1A} UNTIL EQUILIBRIUM IS RE-ESTABLISHED @ $V_{OUT} = 0V$.

AT BIAS POINT $V_{SG} = +1V$.
 $I_{D1} = I_{D2}$
 $= (1/2)(29/R_S)$

IF ONE CURRENT INCREASES THE OTHER MUST DECREASE. SINCE GATES OF Q_{1A} & Q_{1B} ALWAYS REMAIN AT GROUND THE VOLTAGE ACROSS " R_S " REMAINS NEARLY CONSTANT MAKING THIS APPEAR AS A CONSTANT CURRENT SOURCE. SOME CIRCUITS USE ALTERNATE CIRCUITS TO MORE CLOSELY APPROXIMATE THE CONSTANT SOURCE.

OVER THE RANGE OF LINEAR OPERATION $V_{D1} = V_{D2}$ WHICH IS NEARLY EQUAL TO THE SAME LEVEL AS IT IS WITH $0V$ INPUT. FOR ANY INPUT VOLTAGE IN THIS RANGE THE OUTPUT VOLTAGE WILL BE DRIVEN TO $-V_{IN}(R_F/R_I)$, THE RATIO NEEDED TO KEEP $V_{G1A} = 0V$, SINCE GATE CURRENT OF Q_{1A} IS INSIGNIFICANT.

BASIC OPERATIONAL AMPLIFIER REF. (FIGURE TMX-2)

THE FOLLOWING CIRCUITS HAVE MODIFICATIONS WHICH INCLUDE
(COMPONENTS) BUT THE BASIC CIRCUIT STILL HAS THE SAME OPERATION

OPERATION

THE FOLLOWING ASSUMPTIONS ARE MADE:

1. CIRCUIT ADJUSTED FOR $V_{OUT} = 0V$ WHEN $V_{IN} = 0V$ (ADJUSTMENT CIRCUIT NOT SHOWN).
2. Q_{1A} AND Q_{1B} ARE MATCHED WITH CLOSE V_{BE} & BIAS POINT.
3. V_{BE} APPROXIMATELY $= +1V$.
4. SINCE $Q_{1B} = Q_{1A} = 0V$.
5. $I_{D1} = I_{D2}$ (FETS ARE MATCHED PAIR).
6. Q_{2A} & Q_{2B} ARE MATCHED PAIR.
7. SINCE $V_{BA} = V_{BB} = -V_{BE} = -1V$ MAKING $V_{OUT} = 0V$.

IF V_{OUT} STARTS TO GO POSITIVE, THIS (+) VOLTAGE IS FED BACK TO Q_{1A} GATE THRU R_F . THIS RESULTS IN A GREATER VOLTAGE DROP ACROSS R_{D1} THAN R_{D2} MAKING THE DRAIN VOLTAGE OF Q_{1A} (ALSO Q_{2A} BASE VOLTAGE) MORE NEGATIVE THAN THE DRAIN VOLTAGE OF Q_{1B} (ALSO Q_{2B} BASE VOLTAGE). THIS BIAS CONDITION CAUSES Q_{2B} TO CONDUCT MORE AND Q_{2A} TO CONDUCT LESS. Q_{2A} COLLECTOR DOES MORE NEGATIVE MAKING EMITTER FOLLOWER. Q_{2A} EMITTER MORE NEGATIVE. THIS NEGATIVE GOING OUTPUT IS FED BACK THRU R_F TO THE GATE OF Q_{1A} UNTIL EQUILIBRIUM IS RE-ESTABLISHED & $V_{OUT} = 0V$.

$$\begin{aligned} \text{AT BIAS POINT } V_{BE} &= +1V \\ I_{D1} &= I_{D2} \\ &= (1/2)(25\mu A) \end{aligned}$$

THE CIRCUIT IS DESIGNED TO OPERATE WITH $V_{BE} = 1V$. Q_{1A} & Q_{1B} ALWAYS REMAIN AT GROUND THE VOLTAGE ACROSS R_{D1} REMAINS NEARLY CONSTANT MAKING THIS APPEAR AS A CONSTANT CURRENT SOURCE. Q_{2A} & Q_{2B} USE ALTERNATE CIRCUITS TO MORE CLOSELY APPROXIMATE THE CONSTANT SOURCE.

THE CIRCUIT IS DESIGNED TO OPERATE WITH $V_{BE} = 1V$. Q_{1A} & Q_{1B} ALWAYS REMAIN AT GROUND THE VOLTAGE ACROSS R_{D1} REMAINS NEARLY CONSTANT MAKING THIS APPEAR AS A CONSTANT CURRENT SOURCE. Q_{2A} & Q_{2B} USE ALTERNATE CIRCUITS TO MORE CLOSELY APPROXIMATE THE CONSTANT SOURCE.

SAMPLE-AND-HOLD
OPERATION AND TROUBLE-SHOOTING

FIGURE TMX-2 SHOWS A BLOCK DIAGRAM OF THE SAMPLE-AND-HOLD USED IN THIS SYSTEM. THE INPUT AMPLIFIER IS USED IN A SINGLE-ENDED CONFIGURATION WITH INPUT LO GROUNDED. THE FOLLOWING AMPLIFIER IS USED TO SCALE THE FULL-SCALE FROM $\pm 10.24\text{V}$ TO $\pm 10\text{V}$ WHICH IS REQUIRED BY THE ADC. THE OUTPUT OF THIS AMP IS CALLED THE "MD" OR SAMPLE AMP OUT AND IS INVERTED FROM THE INPUT POLARITY.

THE FOLLOWING "HOLD" AMP IS AGAIN INVERTING WHICH MAKES THE OUTPUT OF THE S-H IN PHASE WITH THE INPUT. THIS OUTPUT GOES TO THE ADC INPUT AND IS REFERRED TO AS THE "HOLD" OUTPUT. WHEN THE S-H IS SWITCHED TO "HOLD" THE "MD" OUTPUT IS DISCONNECTED FROM THE S-H INPUT BUT THE "HOLD" CAPACITOR STILL HAS A CHARGE EQUAL TO THE OUTPUT AT THIS TIME. THE DECREASE OF THIS VOLTAGE WITH TIME WHEN THE S-H IS KEPT IN "HOLD" IS CALLED THE "DROOP".

THE TIME THE S-H STAYS IN "HOLD" IN THIS SYSTEM IS SO SHORT THAT THE "DROOP" DOES NOT YIELD ANY MEASURABLE ERROR. IF THE S-H WERE KEPT IN THE "HOLD" MODE FOR A LONG TIME (MINUTES) THE OUTPUT WOULD DRIFT INTO NEGATIVE LOCK-UP (CLAMP LEVEL BEYOND -FS). THIS IS A CHARACTERISTIC OF THIS MODEL S-H.

THE ADC TIMING CONTROLS THE SAMPLE-AND-HOLD SEQUENCE SO THE S-H CANNOT REMAIN IN HOLDS UNLESS OF A MALFUNCTION.

S-H TROUBLE-SHOOTING

THE S-H CAN BE PLACED ON AN EXTENDER CARD SO SAMPLE "SAMPLE" AND "HOLD" COMMANDS CAN BE MONITORED WITH A SCOPE. THE OUTPUT OF IC U2 (PIN-8) SHOULD GO HI WHEN THE "SAMPLE" PULSE IS RECEIVED AND RETURN LO WHEN THE "HOLD" PULSE ARRIVES. IF NOT, THE IC IS PROBABLY BAD. AS IN ANY ELECTRONIC CIRCUIT IT IS ADVISABLE TO CHECK POWER SUPPLIES BEFORE REPLACING THE IC.

THE QUICKEST WAY TO CHECK AN ANALOG PROBLEM IS TO CHECK THE "MD" TP TO DETERMINE WHICH AMP IS BAD. THIS VOLTAGE SHOULD FOLLOW THE INPUT WITH A GAIN DECREASE OF $(-1/1.024)$. AN OFFSET AT THIS POINT OF NO GREATER THAN $\pm 30\text{mV}$ MAY BE NORMAL SINCE THIS AMP IS USED TO COMPENSATE FOR ANY OFFSET IN THE "HOLD" AMP.

IF BAD AT THE "MD" TP CHECK THE OUTPUT OF THE DIFFERENTIAL STAGE TO VERIFY THIS IS EQUAL TO THE INPUT. FIGURE TMX-6 SHOWS A PARTIAL SCHEMATIC OF THE DIFFERENTIAL STAGE. IF THE "MD" IS OK THE PROBLEM IS IN THE "HOLD" AMP OR IN THE LOGIC CIRCUITRY SWITCHING THE BRIDGE. IT IS NOT EASY TO DETERMINE WHICH IS THE CAUSE.

SAMPLE-AND-HOLD OPERATION AND TROUBLE-SHOOTING

FIGURE TMS-2 SHOWS A BLOCK DIAGRAM OF THE SAMPLE-AND-HOLD USED IN THIS SYSTEM. THE INPUT AMPLIFIER IS USED IN A SINGLE-END CONFIGURATION WITH INPUT TO GROUND. THE FOLLOWING AMPLIFIER IS USED TO SCALE THE FULL-SCALE FROM ± 10 V TO ± 10 V WHICH IS REQUIRED BY THE ADC. THE OUTPUT OF THIS AMP IS CALLED THE "MD" OR SAMPLE AMP OUT AND IS INVERTED FROM THE INPUT POLARITY.

THE FOLLOWING "HOLD" AMP IS AGAIN INVERTING WHICH MAKES THE OUTPUT OF THE S-H IN PHASE WITH THE INPUT. THIS OUTPUT GOES TO THE ADC INPUT AND IS REFERRED TO AS THE "HOLD" OUTPUT. WHEN THE S-H IS SWITCHED TO "HOLD" THE "MD" OUTPUT IS DISCONNECTED FROM THE S-H INPUT BUT THE "HOLD" CAPACITOR STILL HAS A CHARGE EQUAL TO THE OUTPUT AT THIS TIME. THE DECREASE OF THIS VOLTAGE WITH TIME WHEN THE S-H IS KEPT IN "HOLD" IS CALLED THE "DROOP".

THE TIME THE S-H STAYS IN "HOLD" IN THIS SYSTEM IS SO SHORT THAT THE "DROOP" DOES NOT YIELD ANY MEASURABLE ERROR. IF THE S-H WERE KEPT IN "HOLD" FOR A LONG TIME (MINUTES), THE OUTPUT WOULD DRIFT INTO NEGATIVE LOCK-UP (CLAMP LEVEL BEYOND -FS). THIS IS A CHARACTERISTIC OF THIS MODEL S-H.

THE ADC TIMING CONTROLS THE SAMPLE-AND-HOLD SEQUENCE SO THE S-H CANNOT BE KEPT IN "HOLD" UNLESS OF A MALFUNCTION.

S-H TROUBLE-SHOOTING

THE S-H CAN BE PLACED ON AN EXTENDER CARD SO SAMPLE "SAMPLE" AND "HOLD" COMMANDS CAN BE MONITORED WITH A SCOPE. THE OUTPUT OF IC U4PIN-8 (SHOULD G) HI WHEN THE "SAMPLE" PULSE IS RECEIVED AND RETURN TO WHEN THE "HOLD" PULSE ARRIVES. IF NOT, THE IC IS PROBABLY BAD. AS IN ANY ELECTRONIC CIRCUIT IT IS ADVISABLE TO CHECK POWER SUPPLIES BEFORE REPAIRING THE IC.

THE QUICKEST WAY TO CHECK AN ANALOG PROBLEM IS TO CHECK THE "MD". IF TO DETERMINE WHICH AMP IS BAD, THIS VOLTAGE SHOULD FOLLOW THE INPUT WITH A GAIN DECREASE OF $(-1/0.04)$. AN OFFSET AT THIS POINT OR NO GREATER THAN ± 10 MVM MAY BE NORMAL SINCE THIS AMP IS USED TO COMPENSATE FOR ANY OFFSET IN THE "HOLD" AMP.

IF BAD AT THE "MD" TO CHECK THE OUTPUT OF THE DIFFERENTIAL STAGE TO VERIFY THIS IS EQUAL TO THE INPUT. FIGURE TMS-2 SHOWS A PARTIAL SCHEMATIC OF THE DIFFERENTIAL STAGE. IF THE "MD" IS ON THE PROBLEM IS IN THE "HOLD" AMP OR IN THE LOGIC CIRCUITRY SWITCHING THE DROOP. IT IS NOT EASY TO DETERMINE WHICH IS THE CAUSE.

THE FOLLOWING TEST IS USED TO RAPIDLY LOCATE THE PROBLEM.

REMOVE GATE OF INPUT FET IN "HOLD" AMP FROM POST AND CONNECT A PAIR OF 1K OHM RESISTORS IN SERIES FROM THE "MD" TO THE "SH" OUT TEST POINTS WITH THE CENTER TIED TO THE FET GATE. THIS REQUIRES UNSOLDERING BUT THE TIME SPENT FOR ON THIS USUALLY SAVES TROUBLE-SHOOTING TIME. THIS CONVERTS THE "HOLD" AMP INTO A STANDARD OP-AMP WITH A GAIN OF -1. THE OUTPUT SHOULD NOW TRACK THE OUTPUT OF THE "MD" (INVERTED). IF THE PROBLEM IS STILL PRESENT THE PROBLEM IS IN THE AMP CIRCUITRY, IF NOT THE PROBLEM IS IN THE LOGIC.

FOR TYPICAL AMP CIRCUIT OPERATION REFER TO FIGURE TMX-2. FOR A DIGITAL PROBLEM REFER TO FIGURE TMX-17.

NOTE: SINCE NEITHER SCHEMATICS NOR ASSEMBLIES HAVE REFERENCE DESIGNATORS FOR ALL COMPONENTS A DETAILED STUDY OF THE CARD WILL BE NEEDED TO LOCATE POINTS TO BE MEASURED.

THE FOLLOWING TEST IS USED TO RAPIDLY LOCATE THE PROBLEM.

REMOVE GATE OF INPUT FET IN "HOLD" AMP FROM POST AND CONNECT A PAIR OF 1K OHM RESISTORS IN SERIES FROM THE "MD" TO THE "SM" OUT TEST POINTS WITH THE CENTER TIED TO THE FET GATE. THIS RESISTOR UNLOADS THE TIME SPENT FOR ON THIS USUALLY SAVES TROUBLE-SHOOTING TIME. CONVERTS THE "HOLD" AMP INTO A STANDARD OP-AMP WITH A GAIN OF -1. THE OUTPUT SHOULD NOW TRACK THE OUTPUT OF THE "MD" (INVERTED). IF THE PROBLEM IS STILL PRESENT THE PROBLEM IS IN THE AMP CIRCUITRY. IF NOT THE PROBLEM IS IN THE LOGIC.

FOR TYPICAL AMP CIRCUIT OPERATION REFER TO FIGURE TMX-2. FOR A DIGITAL PROBLEM REFER TO FIGURE TMX-17.

NOTE: SINCE NEITHER SCHEMATICS NOR ASSEMBLIES HAVE REFERENCE DESIGNATORS FOR ALL COMPONENTS A DETAILED STUDY OF THE CARD WILL BE NEEDED TO LOCATE POINTS TO BE MEASURED.

FET USES

FETS ARE USED IN THREE WAYS THROUGHOUT THIS SYSTEM.

- 1 AMPLIFIER INPUTS
- 2 MULTIPLEXER SWITCHES
- 3 CONSTANT CURRENT SOURCES

AMPLIFIER INPUTS:

FETS ARE USED FOR HIGH INPUT IMPEDANCE AND BIASED IN THE LINEAR REGION WITH I_D USUALLY BETWEEN .1 AND 1 MA. FOR MOST CIRCUITS THEY ARE USED AS MATCHED PAIRS.

MULTIPLEXER SWITCHES:

MULTIPLEXER INPUTS ARE CONTROLLED BY GATE BIAS AS SHOWN IN FIGURE TMX-14.

WITH CONTROL INPUT AT -20V THE GATE TO SOURCE IS MAINTAINED MORE NEGATIVE THAN V_P FOR THE MOST NEGATIVE INPUT. THIS KEEPS THE FET OFF. TO TURN THE FET ON THE CONTROL INPUT GOES TO +20V WHICH BACK BIASES THE DIODE SHOWN AND ALLOWS THE VOLTAGE GATE - SOURCE TO BE 0V. SINCE THE "ON" RESISTANCE OF THE FET IS NOMINALLY 200 OHMS A HIGH IMPEDANCE BUFFER OR S-H MUST BE USED TO FOLLOW THIS SWITCH.

CONSTANT CURRENT SOURCES:

FETS ARE SELECTED FOR $I_{DSS} = 3$ TO 5MA.

THESE FETS ARE USED IN SERIES WITH ZENER DIODE POWER SUPPLIES ON CIRCUIT CARDS. THE FETS MAINTAIN A MORE CONSTANT CURRENT THAN A SERIES RESISTOR WITH A CHANGING INPUT VOLTAGE. (REF FIG. TMX-15)

****FET USED****

FETS ARE USED IN THREE WAYS THROUGHOUT THIS SYSTEM.

1. AMPLIFIER INPUTS
2. MULTIPLEXER SWITCHES
3. CONSTANT CURRENT SOURCES

AMPLIFIER INPUTS

FETS ARE USED FOR HIGH INPUT IMPEDANCE AND BIASED IN THE LINEAR REGION WITH ID USUALLY BETWEEN .1 AND 1 MA. FOR FET CIRCUITS THEY ARE USED AS MATCHED PAIRS.

MULTIPLEXER SWITCHES

MULTIPLEXER INPUTS ARE CONTROLLED BY GATE BIAS AS SHOWN IN FIGURE TMX-1A.

WITH CONTROL INPUT AT -20V THE GATE TO SOURCE IS MAINTAINED MORE NEGATIVE THAN VP FOR THE MOST NEGATIVE INPUT. THIS KEEPS THE FET OFF TO TURN THE FET ON THE CONTROL INPUT GOES TO +20V WHICH BACK BIASES THE DIODE SHOWN AND ALLOWS THE VOLTAGE GATE - SOURCE TO BE 0V. SINCE THE "ON" RESISTANCE OF THE FET IS NOMINALLY 200 OHMS A HIGH IMPEDANCE BUFFER OR S-H MUST BE USED TO FOLLOW THIS SWITCH.

CONSTANT CURRENT SOURCES

FETS ARE SELECTED FOR $I_{DSS} = 3$ TO 5 MA.

A SERIES RESISTOR WITH A CHANGING INPUT VOLTAGE (REF FIG. TMX-1B) MUST BE USED. THE FET BEHAVIOR A LONG CHANNEL TRANSISTOR IS USED.

*** AMP-LOGIC BOARD OPERATION ***

A POSITIVE "ANALOG" INPUT VOLTAGE (VIN) WILL DRIVE THE "POS" AMP OUTPUT IN A "POSITIVE" DIRECTION AND THE "NEG" AMP OUTPUT IN A "NEGATIVE" DIRECTION. THIS WILL BIAS Q7 "ON" AND Q8 "OFF". THE "ANALOG" OUTPUT (VOUT) OF THE BOARD WILL BE DEPENDENT UPON THE MAGNITUDE OF THE "POS" AMP OUTPUT ONLY.

IN THE LINEAR REGION OF OPERATION THE (+) AND (-) INPUTS OF THE "POS" AMP WILL BE NEARLY AT THE SAME VOLTAGE, (VIN). THIS PRODUCES A CURRENT OF $(10 - VIN)/(4K)$ FROM THE +10 REF TO THE JUNCTION OF THE "POS" AMP (-) INPUT. SINCE NO CURRENT FLOWS INTO THE (-) INPUT THIS CURRENT ALL FLOWS THRU THE 4008 OHM RESISTOR TO THE OUTPUT. THUS THE "ANALOG" OUTPUT (VOUT) IS EQUAL TO:

$$\begin{aligned} (VOUT) &= (VIN) - (10 - VIN)/(4K)*(4008) \\ (VOUT) &= 2(VIN) - 10 \quad \text{APPROXIMATELY} \end{aligned}$$

A "NEGATIVE" ANALOG INPUT VOLTAGE WILL DRIVE THE "NEG" AMP OUTPUT IN A "POSITIVE" DIRECTION AND THE "POS" AMP OUTPUT IN A "NEGATIVE" DIRECTION. THIS WILL BIAS Q8 "ON" AND Q7 "OFF". THE ANALOG OUTPUT THE BOARD WILL BE DEPENDENT UPON THE MAGNITUDE OF THE "NEG" AMP OUTPUT ONLY.

THIS IS AN OPERATIONAL AMPLIFIER WITH:

$$\begin{aligned} (VOUT) &= -(+10)(8000/8038) - (-VIN)(8000/4008) \\ (VOUT) &= -10 + 2(VIN) \quad \text{APPROXIMATELY} \end{aligned}$$

THIS IS THE SAME OUTPUT AS OBTAINED WITH A POSITIVE INPUT USING THE "POS" AMP.

THE POLARITY OF THE VOLTAGE DROP BETWEEN Q7C AND Q8C DEPENDS UPON WHICH TRANSISTOR IS CONDUCTING SINCE THE COLLECTOR OF THE "ON" TRANSIS "NEGATIVE" WITH RESPECT TO THE COLLECTOR OF THE "OFF" TRANSISTOR. THIS DIFFERENCE IS APPLIED TO THE INPUTS OF THE VOLTAGE COMPARATOR IC WHICH DETERMINES THE DIGITAL OUTPUT OF THE BOARD.

AMP-LOGIC "A" P/N 56620
AMP-LOGIC "A-B" P/N 46000
AMP-LOGIC "B" P/N 46023
AMP-LOGIC "C" P/N 46016

THESE BOARDS HAVE THE SAME TRANSFER FUNCTION AS THE AMP-LOGIC "A" P/N 52640 BUT USE DIFFERENT CIRCUITRY. FIGURE TMX-5 SHOWS A BLOCK DIAGRAM WITH RATIOS FOR GAIN RELATED RESISTORS.

*** AMP-LOGIC BOARD OPERATION ***

A POSITIVE "ANALOG" INPUT VOLTAGE (VIN) WILL DRIVE THE "POS" AMP OUTPUT IN A "POSITIVE" DIRECTION AND THE "NEG" AMP OUTPUT IN A "NEGATIVE" DIRECTION. THIS WILL BIAS Q7 "ON" AND Q8 "OFF". THE "ANALOG" OUTPUT (VOUT) OF THE BOARD WILL BE DEPENDENT UPON THE MAGNITUDE OF THE "POS" AMP OUTPUT ONLY.

IN THE LINEAR REGION OF OPERATION THE (+) AND (-) INPUTS OF THE "POS" AMP WILL BE NEARLY AT THE SAME VOLTAGE (VIN). THIS PRODUCES A CURRENT OF $(10 - VIN) / (AK)$ FROM THE +10 REF TO THE JUNCTION OF THE "POS" AMP (-) INPUT. SINCE NO CURRENT FLOWS INTO THE (-) INPUT THIS CURRENT ALL FLOWS THRU THE 4008 OHM RESISTOR TO THE OUTPUT. THUS THE "ANALOG" OUTPUT (VOUT) IS EQUAL TO:

$$(VOUT) = (VIN) - (10 - VIN) / (AK) * (4008) \\ (VOUT) = 2(VIN) - 10 \text{ APPROXIMATELY}$$

A "NEGATIVE" ANALOG INPUT VOLTAGE WILL DRIVE THE "NEG" AMP OUTPUT IN A "POSITIVE" DIRECTION AND THE "POS" AMP OUTPUT IN A "NEGATIVE" DIRECTION. THIS WILL BIAS Q8 "ON" AND Q7 "OFF". THE ANALOG OUTPUT OF THE BOARD WILL BE DEPENDENT UPON THE MAGNITUDE OF THE "NEG" AMP OUTPUT ONLY.

THIS IS AN OPERATIONAL AMPLIFIER WITH:

$$(VOUT) = -((+10) / (8000 / (8000 / (4008))) * (-VIN) / (8000 / (4008))) \\ (VOUT) = -10 + 2(VIN) \text{ APPROXIMATELY}$$

THIS IS THE SAME OUTPUT AS OBTAINED WITH A POSITIVE INPUT USING THE "POS" AMP.

THE POLARITY OF THE VOLTAGE DROP BETWEEN Q7C AND Q8C DEPENDS UPON WHICH TRANSISTOR IS CONDUCTING SINCE THE COLLECTOR OF THE "ON" TRANSISTOR "NEGATIVE" WITH RESPECT TO THE COLLECTOR OF THE "OFF" TRANSISTOR. THIS DIFFERENCE IS APPLIED TO THE INPUTS OF THE VOLTAGE COMPARATOR IC WHICH DETERMINES THE DIGITAL OUTPUT OF THE BOARD.

AMP-LOGIC "A" P/N 56620
AMP-LOGIC "A-B" P/N 45000
AMP-LOGIC "B" P/N 46023
AMP-LOGIC "C" P/N 45016

FIGURE 1-10: AMP-LOGIC BOARD OPERATION. BUT USE DIFFERENT CIRCUITRY. FIGURE 1-11: AMP-LOGIC BOARD OPERATION. WITH RATIOS FOR GAIN RELATED RESISTORS.

WITH A "NEGATIVE" ANALOG INPUT VOLTAGE THE FIRST AMP OUTPUT GOES "POSITIVE" AND IS COUPLED TO THE SUMMING POINT OF THE SECOND AMP BY ONLY A LARGE VALUE RESISTOR FOR TRIMMING PURPOSES. THE ANALOG IS ALSO COUPLED DIRECTLY TO THE SUMMING POINT THRU A RESISTOR WITH A VALUE OF $1/2 R_F$. THE +10 REF IS COUPLED INTO THE SUMMING JUNCTION WITH A RESISTOR OF NOMINALLY R_F . THEREFORE:

$$\begin{aligned}(V_{OUT}) &= -(-V_{IN})(R_F/(R_F/2)) - 10(R_F/R_F) \\(V_{OUT}) &= 2(V_{IN}) - 10\end{aligned}$$

WITH A POSITIVE INPUT THE FIRST AMP GOES NEGATIVE. THE INVERTED INPUT IS THUS FED TO THE SUMMING JUNCTION THRU A RESISTOR OF $R_F/4$.

$$\begin{aligned}(V_{OUT}) &= -(-V_{IN})(R_F/(R_F/4)) - V_{IN}(R_F/(R_F/2)) - 10(R_F/R_F) \\(V_{OUT}) &= 4(V_{IN}) - 2(V_{IN}) - 10 \\(V_{OUT}) &= 2(V_{IN}) - 10\end{aligned}$$

THE SAME AS FOR THE OUTPUT WITH A NEGATIVE VOLTAGE.

THE "POLARITY" OF OUTPUT IS USED TO SWITCH THE LOGIC WHICH DETERMINES THE DIGITAL OUTPUT OF THE BOARD.

WITH A "NEGATIVE" ANALOG INPUT VOLTAGE THE FIRST AMP OUTPUT GOES
 "POSITIVE" AND IS COUPLED TO THE SUMMING POINT OF THE SECOND AMP BY
 ONLY A LARGE VALUE RESISTOR FOR TRIMMING PURPOSES. THE ANALOG IS ALSO
 COUPLED DIRECTLY TO THE SUMMING POINT THRU A RESISTOR WITH A VALUE OF
 1K2. THE +10 REF IS COUPLED INTO THE SUMMING JUNCTION WITH A
 RESISTOR OF NOMINALLY 1K. THEREFORE:

$$\begin{aligned} (VOUT) &= -(-VIN)(REF/REFS) - 10(REF/REF) \\ (VOUT) &= 2(VIN) - 10 \end{aligned}$$

WITH A POSITIVE INPUT THE FIRST AMP GOES NEGATIVE. THE INVERTED INPUT
 IS THUS FED TO THE SUMMING JUNCTION THRU A RESISTOR OF 1K2.

$$\begin{aligned} (VOUT) &= -(-VIN)(REF/REFS) - VIN(REF/REFS) - 10(REF/REF) \\ (VOUT) &= 4(VIN) - 2(VIN) - 10 \\ (VOUT) &= 2(VIN) - 10 \end{aligned}$$

THE SAME AS FOR THE OUTPUT WITH A NEGATIVE VOLTAGE.

THE "POLARITY" OUTPUT IS USED TO SWITCH THE LOGIC WHICH DETERMINES
 THE DIGITAL OUTPUT OF THE BOARD.

CALIBRATION

BEFORE PERFORMING ANY CALIBRATION ON THE SYSTEM IT IS RECOMMENDED THAT AN ADEQUATE CHECK BE MADE FIRST TO VERIFY THAT CALIBRATION IS REQUIRED. IF IT IS, IT MUST BE PERFORMED UNDER CONTROLLED CONDITIONS AND WITH PROPER TEST EQUIPMENT. TO EVEN VERIFY THAT CALIBRATION IS NEEDED MAY REQUIRE THE SAME EQUIPMENT AND CONTROLS WHICH INCLUDE:

1) THE UNIT MUST BE THOROUGHLY WARMED UP AND OPERATING AT A STABLE TEMPERATURE OF APPROXIMATELY 25 DEGREES C.

2) A CALIBRATED VOLTAGE SOURCE (JOHN FLUKE MODEL 343A) OR EQUIVALENT MUST BE AVAILABLE.

3) A PRESTON CALIBRATION COVER OR EQUIVALENT MUST BE AVAILABLE.

4) THE UNIT CAN BE RUN ON THE INTERNAL HI-SPEED CLOCK BUT THE FOLLOWING JUMPERS ARE STILL REQUIRED:

J2-52	-----	J2-54
J2-60	-----	J2-80

5) ALL ANALOG INPUT CHANNELS MUST BE WIRED SO THEY CAN EITHER BE CONNECTED TO THE CALIBRATOR OR TO GND.

AFTER A 1 HOUR MINIMUM WARM-UP PERIOD THE CALIBRATOR SHOULD BE USED TO APPLY VOLTAGES AS REQUIRED TO PRODUCE CODES REQUIRED BY 32 POINT LINEARITY SHEET (FIG TMX-13). THIS SHOULD BE DONE WITH THE MUX ADDRESS AT CH4 IN THE RANDOM CONTINUOUS MODE. BY USING THIS FET-MUX CHANNEL THE ERROR SOURCES SUCH AS ZERO OFFSET, GAIN, AND NON-LINEARITY ARE ELIMINATED. WHEN THE SYSTEM CALIBRATION THRU CH4 IS COMPLETE THE AMP-MUX CHANNELS CAN BE COMPARED AND THE CORRESPONDING ZERO AND GAIN ADJUSTMENTS CAN BE TOUCHED UP, IF NECESSARY.

REMOTE SENSE LINES ARE NOT REQUIRED WHEN PUTTING INPUT ON CH4 BUT WILL BE NEEDED IF USING AN ARRANGEMENT SUCH AS SHOWN ON FIG TMX-9 BECAUSE THE ATTENUATORS ARE LOW IMPEDANCE LOADS ON THE SOURCE.

WHEN THE DATA FOR THE LINEARITY CHECK HAS BEEN RECORDED A LINEARITY CURVE CAN BE PLOTTED TO DETERMINE IF A RE-CALIBRATION IS REQUIRED. THE PROCEDURE FOR PLOTTING THE LINEARITY CURVE IS DETAILED IN SECTION 6 OF THE MANUAL AND WILL ONLY BE SUMMARIZED HERE. BRIEFLY, THE DIFFERENCE BETWEEN THE THEORETICAL AND ACTUAL INPUTS (IN MV) IS PLOTTED AS AN ERROR. THE ALGEBRAIC SIGN MUST BE INCLUDED. POINTS MUST BE PLOTTED IN THE EXACT SEQUENCE WHICH THEY WERE TAKEN. EXCEPT FOR FULL-SCALES, THE VALUES ARE GROUPED IN PAIRS, ONE ON EACH SIDE OF THE ACTUAL MAJOR BIT ABOUT WHICH THE TRANSITION POINTS WERE TAKEN. THESE PAIRS OF POINTS ARE PLOTTED ON THE SAME HORIZONTAL LOCATION. IF AN EXPANDED SCALE WAS USED THE FIRST ONE WOULD BE SLIGHTLY AHEAD OF THE SECOND BUT THIS DIFFERENCE

RE-CALIBRATION

AN ADEQUATE CHECK BE MADE FIRST TO VERIFY THAT CALIBRATION IS REQUIRED. IF IT IS, IT MUST BE PERFORMED UNDER CONTROLLED CONDITIONS AND WITH PROPER TEST EQUIPMENT TO EVEN VERIFY THAT CALIBRATION IS NEEDED MAY REQUIRE THE SAME EQUIPMENT AND CONTROLS WHICH INCLUDE:

- 1) THE UNIT MUST BE THOROUGHLY WARMED UP AND OPERATING AT A STABLE TEMPERATURE OF APPROXIMATELY 25 DEGREES C.
- 2) A CALIBRATED VOLTAGE SOURCE (JOHN FLUKE MODEL 343A) OR EQUIVALENT MUST BE AVAILABLE
- 3) A PRESTON CALIBRATION COVER OR EQUIVALENT MUST BE AVAILABLE.

- 4) THE UNIT CAN BE RUN ON THE INTERNAL HI-SPEED CLOCK BUT THE FOLLOWING NUMBERS ARE STILL REQUIRED:
- | | |
|-------|-------|
| 05-80 | 05-80 |
| 05-80 | 05-80 |
| 05-80 | 05-80 |

- 5) ALL ANALOG INPUT CHANNELS MUST BE WIRED SO THEY CAN EITHER BE CONNECTED TO THE CALIBRATOR OR TO GND.
- AFTER A 1 HOUR MINIMUM WARM-UP PERIOD THE CALIBRATOR SHOULD BE USED TO APPLY VOLTAGES AS REQUIRED TO PRODUCE CODES REQUIRED BY 3C POINT LINEARITY SHEET (FIG TMX-13). THIS SHOULD BE DONE WITH THE MAX ADDRESS AT CHA IN THE RANDOM CONTINUOUS MODE. BY USING THIS PFMUX CHANNEL THE ERROR SOURCES SUCH AS ZERO OFFSET, GAIN, AND NON-LINEARITY ARE ELIMINATED. WHEN THE SYSTEM CALIBRATION THRU CHA IS COMPLETE THE PFMUX CHANNELS CAN BE COMPARED AND THE CORRESPONDING ZERO AND GAIN ADJUSTMENTS CAN BE TOUCHED UP, IF NECESSARY.

REMOTE SENSE LINES ARE NOT REQUIRED WHEN POTTING INPUT ON CHA BUT WILL BE NEEDED IF USING AN ARRANGEMENT SUCH AS SHOWN ON FIG TMX-9 BECAUSE THE ATTENUATORS ARE LOW IMPEDANCE LOADS ON THE SOURCE.

WHEN THE DATA FOR THE LINEARITY CHECK HAS BEEN RECORDED A LINEARITY CURVE CAN BE PLOTTED TO DETERMINE IF A RE-CALIBRATION IS REQUIRED. THE PROCEDURE FOR PLOTTING THE LINEARITY CURVE IS DETAILLED IN SECTION 6 OF THE MANUAL AND WILL ONLY BE SUMMARIZED HERE. BRIEFLY, THE DIFFERENCE BETWEEN THE THEORETICAL AND ACTUAL INPUTS (IN MV) IS PLOTTED AS AN ERROR. THE ALGEBRAIC SIGN MUST BE INCLUDED. POINTS MUST BE PLOTTED IN THE EXACT SEQUENCE WHICH THEY WERE TAKEN. EXCEPT FOR PFMUX CHANNELS, ALL VALUES ARE GROUPED IN PAIRS, ONE ON EACH SIDE OF THE ACTUAL MAJOR 0.1 VOLTAGE. THE PFMUX CHANNELS MUST BE TAKEN FIRST. THE DATA SHOULD BE PLOTTED ON THE SAME HORIZONTAL LOCATION. IF AN EXPANDED SCALE WAS USED, THE FIRST ONE WOULD BE SLIGHTLY AHEAD OF THE SECOND BUT THIS DIFFERENCE

IS NOT NOTICABLE ON THE SCALE USED. FOR PRACTICAL PURPOSES A 1 MV/DIV VERTICAL ON A STANDARD QUAD PAD WITH 1/4 INCH INCREMENTS IS ADEQUATE. THIS IS COMPATIBLE WITH NORMAL REPEATABILITY.

FIGURES 90029 THRU 90045 OF THE MANUAL SHOW TYPICAL PLOTS BASED ON NUMBERS CORRESPONDING TO A $\pm 10V$ SYSTEM. THIS APPLIES TO THE ADC WITHOUT THE S-H. SINCE THIS SYSTEM IS $\pm 10.24VFS$ ON MULTIPLEXER CHANNELS WITHOUT AMPS THE ACTUAL NUMBERS FOR CALIBRATION THRU CH4 ARE CLOSE BUT DIFFERENT. REFER TO FIGTMX-13 .

THE IMPORTANT INFORMATION SHOWN ON THE LINEARITY CURVE IS:

OVERALL OFFSET ERROR
OVERALL GAIN ERROR
LINEARITY
TRANSITION WIDTHS
*** OFFSET ***

AN OFFSET MAY BE CORRECTED BY FP ADJUSTMENT BUT ALL OTHER ADJUSTMENTS ARE INTERNAL. IF, AFTER ANALYZING THE LINEARITY PLOT A CALIBRATION OR TOUCH-UP IS REQUIRED THE PRESTON CALIBRATION COVER MUST BE INSTALLED AND THE UNIT MUST BE ALLOWED TIME FOR RE-STABILIZATION. NORMALLY 30 MINUTES IS ADEQUATE. FOR A FACTORY CALIBRATION THE STANDARD PROCEDURE IS TO HAVE THE UNIT RUN OVERNIGHT AND PERFORM THE CALIBRATION THE NEXT DAY.

*** GAIN ***

THE GAIN POT ON THE S-H MAY BE USED TO CORRECT A SMALL GAIN ERROR ($\pm$ A FEW MV) IF THIS IS THE ONLY ERROR TO BE CORRECTED. ANY OFFSET ERRORS SHOULD HAVE BEEN REMOVED FIRST.

*** LINEARITY ***

THIS REFERS TO THE SHAPE OF THE ACTUAL PLOT COMPARED TO THE THEORETICAL PLOT. CORRECTIONS REQUIRE ADJUSTMENTS TO THE ADC AMP-LOGIC CARDS.

*** TRANSITION WIDTHS ***

THIS REFERS TO THE "WIDTHS" OF THE ACTUAL TRANSITIONS AS COMPARED TO THE THEORETICAL "WIDTHS". CORRECTIONS REQUIRE ADJUSTMENT TO ADC CARDS.

13. NOT NOTICABLE ON THE SCALE USED. FOR PRACTICAL PURPOSES A 1 MV/DIV VERTICAL ON A STANDARD GRID WITH 1/4 INCH INCREMENTS IS ADEQUATE. THIS IS COMPATIBLE WITH NORMAL REPEATABILITY.

FIGURES 20002 THRU 20005 OF THE MANUAL SHOW TYPICAL PLOTS BASED ON NUMBERS CORRESPONDING TO A +/- 10V SYSTEM. THIS APPLIES TO THE ADC WITHOUT THE S-H. SINCE THIS SYSTEM IS +/- 10 VOLTS ON MILLIVOLTS CHANNELS WITHOUT AMPS THE ACTUAL NUMBERS FOR CALIBRATION THRU CH4 ARE CLOSE BUT DIFFERENT REFER TO FIGMX-13

THE IMPORTANT INFORMATION SHOWN ON THE LINEARITY CURVE IS

OVERALL OFFSET ERROR
OVERALL GAIN ERROR
LINEARITY
TRANSITION WIDTH
*** OFFSET ***

AN OFFSET MAY BE CORRECTED BY AN ADJUSTMENT BUT ALL OTHER ADJUSTMENTS ARE INTERNAL. AFTER ANALYZING THE LINEARITY PLOT A CALIBRATION OR TOUCH-UP IS REQUIRED. THE PRECISION CALIBRATION COVER MUST BE INSTALLED AND THE UNIT MUST BE ALLOWED TIME FOR RE-STABILIZATION. NORMALLY 30 MINUTES IS ADEQUATE. FOR A FACTORY CALIBRATION THE STANDARD PROCEDURE IS TO HAVE THE UNIT RUN OVERNIGHT AND PERFORM THE CALIBRATION THE NEXT DAY.

*** GAIN ***

THE GAIN PUT ON THE S-H MAY BE USED TO CORRECT A SMALL GAIN ERROR. A SHOULD HAVE BEEN REMOVED FIRST

*** LINEARITY ***

THIS REFERS TO THE SHAPE OF THE ACTUAL PLOT COMPARED TO THE THEORETICAL. CORRECTIONS REQUIRE ADJUSTMENT TO THE ADC AMP-LOGIC CARDS.

*** TRANSITION WIDTH ***

OF THE ACTUAL TRANSITION AS COMPARED TO THE THEORETICAL. CORRECTIONS REQUIRE ADJUSTMENT TO ADC CARDS.

AS STATED IN REFERENCED MANUAL SECTION 6 THE SHAPE OF THE CURVE INCLUDING TRANSITION "WIDTHS" IS IMPORTANT TO BE SURE THE ADC IS MONOTONIC(DIGITAL OUTPUT INCREASES AS ANALOG INPUT INCREASES WITH NO MISSING CODES). THE PRACTICAL "WIDTH" ADJUSTMENTS PUT SOME "EXTRA" WIDTH INTO THE MOST SIGNIFICANT TRANSITIONS TO ALLOW FOR DRIFT DUE TO TEMPERATURE CHANGES OR COMPONENT AGING. THIS SLIGHTLY DEGRADES THE IMMEDIATE CALIBRATION PRECISION BUT IS NECESSARY.

AS STATED IN REFERENCED MANUAL SECTION 6 THE SHAPE OF THE CURVE INCLUDING TRANSITION "WIDTH" IS IMPORTANT TO BE SURE THE ADC IS MONOTONIC(DIGITAL OUTPUT INCREASES AS ANALOG INPUT INCREASES WITH NO MISSING CODES). THE PRACTICAL "WIDTH" ADJUSTMENTS PUT SOME "EXTRA" WIDTH INTO THE MOST SIGNIFICANT TRANSITIONS TO ALLOW FOR DRIFT DUE TO TEMPERATURE CHANGES OR COMPONENT AGING. THIS SLIGHTLY DEGRADES THE IMMEDIATE CALIBRATION PRECISION BUT IS NECESSARY.

*** GENERAL INFORMATION RELATED TO CALIBRATION ***

IF A FEW ADJUSTMENTS ON ADC CARDS CORRECT THE LINEARITY CURVE A COMPLETE CALIBRATION AS OUTLINED IN THE MANUAL IS NOT REQUIRED. EVEN IF COMPLETE RE-CALIBRATION OF SEVERAL ADC CARDS IS REQUIRED IT IS SELDOM NECESSARY TO COMPLETELY RE-CALIBRATE THE ENTIRE ADC.

WHEN CALIBRATING THE ADC ALWAYS USE A FET-MUX CHANNEL INSTEAD OF AN AMP-MUX CHANNEL TO AVOID OFFSET OF GAIN ERRORS INTRODUCED BY THE AMP. THIS CHANNEL MAY THEN BE USED AS A REFERENCE FOR SETTING ZEROS AND GAINS FOR OTHER CHANNELS.

WHEN ZEROS FOR ALL CHANNELS HAVE BEEN ADJUSTED THE MULTIPLEXER MAY BE SET TO CONTINUOUS OPERATION AND SCAN THRU ALL CHANNELS. IF THE OUTPUT OF THE 4 LEAST SIGNIFICANT BITS IS CONNECTED TO A SIMPLE DAC SUCH AS SHOWN ON FIG TMX-20 A COMPARISON OF CHANNELS CAN BE MADE USING A SCOPE TO MONITOR THE DAC OUTPUT. THIS IS ONLY VALID IF ALL ZEROS HAVE BEEN SET TO CLOSE TO FINAL VALUES BECAUSE THE DAC WOULD HAVE THE SAME OUTPUT IF A MORE SIGNIFICANT BIT WAS DIFFERENT. THE SCOPE CAN BE SYNCED ON COIN WHICH IS TRUE DURING LAST CHANNEL. THIS IS A USEFUL AID IN TOUCHING -UP AMP-MUX ZEROS SINCE AMP-MUX CHANNELS MAY BE COMPARED WITH FET-MUX CH WHICH HAVE NO OFFSETS. THIS SAME PROCEDURE MAY BE USED TO TOUCH-UP GAINS BUT CHANNELS MUST FIRST BE GROUPED TO HAVE SAME GAINS OR MULTIPLE CALIBRATORS MUST BE USED. ALLOW SETTLING TIME WHENEVER EVERY TIME A CIRCUIT CARD IS REMOVED OR THE COVER IS REMOVED. OTHERWISE, SETTINGS MADE MAY NOT BE FINAL VALUES. AS A RULE OF THUMB THE FOLLOWING TIMES ARE ADEQUATE FOR ADC CALIBRATION:

AMP-LOGIC CARDS "B" , "C", 4 BIT AMP	5 MINUTES
AMP-LOGIC CARDS "A2" THRU "A5"	30 MINUTES
AMP-LOGIC CARD "A1", SAMPLE-AND-HOLD	60 MINUTES

THE LONGER TIME FOR THE "A1" AND S-H IS REQUIRED BECAUSE OTHER CARDS MAY BE KEPT IN THE BOX RUNNING IN ALTERNATE SLOTS AND ARE ONLY REMOVED TO CHANGE SLOTS.

THE TIME USED FOR STABILIZATION MAY SAVE MUCH MORE TIME SPENT MAKING REPEATED ADJUSTMENTS ON CARDS WHICH WERE SET WHILE NOT SETTLED.

FINAL CALIBRATION IS ALWAYS DONE AS A "SYSTEM" AND IT IS NORMAL THAT A GIVEN SECTION MAY ACTUALLY BE SOMEWHAT "UNCALIBRATED" TO COMPENSATE FOR SOME OTHER SECTION. THEREFORE THE ADC MAY BE CALIBRATED BUT DUE TO A NON-LINEARITY OR OTHER ERROR IN THE S-H MAY APPEAR SLIGHTLY UNCALIBRATED IF CHECKED WITHOUT THE S-H.

THE ADC IS A "SYMMETRICAL" DEVICE IN RESPECT TO THE TRANSITIONS, THAT IS, THE TRANSITION WIDTHS OR OTHER CHARACTERISTICS FOR A GIVEN BIT SUCH AS "DB4096" CORRESPONDING TO THE 1/4 SCALE INCREMENTS SHOULD BE THE SIMILAR AT ALL POINTS PLOTTED(-3/4, -1/4, +1/4, +3/4) SCALE. IF NOT,

*** GENERAL INFORMATION RELATED TO CALIBRATION ***

IF A FEW ADJUSTMENTS ON ADC CARDS CORRECT THE LINEARITY CURVE A COMPLETE CALIBRATION AS OUTLINED IN THE MANUAL IS NOT REQUIRED. EVEN IF COMPLETE RE-CALIBRATION OF SEVERAL ADC CARDS IS REQUIRED IT IS BECOMING NECESSARY TO COMPLETELY RE-CALIBRATE THE ENTIRE ADC.

WHEN CALIBRATING THE ADC ALWAYS USE A FET-MUX CHANNEL INSTEAD OF AN AMP-MUX CHANNEL TO AVOID OFFSET OR GAIN ERRORS INTRODUCED BY THE AMP. THIS CHANNEL MAY THEN BE USED AS A REFERENCE FOR SETTING ZEROS AND GAINS FOR OTHER CHANNELS.

WHEN ZEROS FOR ALL CHANNELS HAVE BEEN ADJUSTED THE MULTIPLIER MAY BE SET TO CONTINUOUS OPERATION AND SCAN THRU ALL CHANNELS. IN THE OUTPUT OF THE 4 LEAST SIGNIFICANT BITS IS CONNECTED TO A SIMPLE DAC SUCH AS SHOWN ON FIG. 1-20. A COMPARISON OF CHANNELS CAN BE MADE USING A SCOPE TO MONITOR THE DAC OUTPUT. THIS IS ONLY VALID IF ALL ZEROS HAVE BEEN SET TO CLOSE TO FINAL VALUES BECAUSE THE DAC WOULD HAVE THE SAME OUTPUT IF A MORE SIGNIFICANT BIT WAS DIFFERENT. THE SCOPE CAN BE SYNCHRONIZED ON A SIGNAL WHICH IS TRUE DURING LAST CHANNEL. THIS IS A USEFUL AID IN CHECKING -UP AMP-MUX ZEROS SINCE AMP-MUX CHANNELS MAY BE COMPARED WITH FET-MUX CH WHICH HAVE NO OFFSETS. THIS SAME PROCEDURE MAY BE USED TO CHECK-UP GAINS BUT CHANNELS MUST FIRST BE GROUPED TO HAVE SAME GAIN. OR MULTIPLE CALIBRATIONS MUST BE USED. ALLOW SETTING TIME WHENEVER EVERY TIME A CIRCUIT CARD IS REMOVED OR THE COVER IS REMOVED. OVERLAPPING SETTINGS MADE MAY NOT BE FINAL VALUES AS A RULE OF THUMB. THE FOLLOWING TIMES ARE ADEQUATE FOR ADC CALIBRATION:

AMP-LOGIC CARDS "B", "C", 4 BIT AMP	5 MINUTES
AMP-LOGIC CARDS "A2" THRU "A5"	30 MINUTES
AMP-LOGIC CARD "A1", SAMPLE-AND-HOLD	60 MINUTES

THE LONGER TIME FOR THE "A1" AND 5-H IS REQUIRED BECAUSE OTHER CARDS MAY BE SET IN THE BOX RUNNING IN ALTERNATE SLOTS AND ARE ONLY REMOVED TO CHANGE SLOTS.

THE TIME USED FOR STABILIZATION MAY SAVE MUCH MORE TIME WHEN MAKING REPEATED ADJUSTMENTS ON CARDS WHICH WERE SET WHILE NOT SETTLED.

FINAL CALIBRATION IS ALWAYS DONE AS A "SYSTEM" AND IT IS NORMAL THAT A GIVEN SECTION MAY ACTUALLY BE SOMEWHAT "UNCALIBRATED" TO COMPENSATE FOR SOME OTHER SECTION. THEREFORE THE ADC MAY BE CALIBRATED BUT DUE TO A NON-LINEARITY OR OTHER ERROR IN THE 5-H MAY APPEAR SLIGHTLY UNCALIBRATED IF CHECKED WITHOUT THE 5-H.

THE ADC IS A "SYMMETRICAL" DEVICE IN RESPECT TO THE TRANSITIONS. THAT IS, THE TRANSITION WIDTHS OR OTHER CHARACTERISTICS FOR A GIVEN BIT SUCH AS "PEAKS" CORRESPONDING TO THE 1-H SCALE INCREMENTS SHOULD BE THE SAME AT ALL POINTS PLOTTED: $(-254, -124, +124, +254)$ SCALE. IF NOT

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CHECK FOR PLOTTING ERROR OR POSSIBLE OSCILLATION IN THE AMP-LOGIC
CARD(A3 FOR DB4096).

A CHANGE IN THE +10V REF WILL CAUSE A CORRESPONDING CHANGE TO THE -10V REF. THE RESULTING -10V CHANGE WILL NOT AFFECT THE ADC BUT WILL CAUSE A ZERO SHIFT IN THE S-H. THE CHANGE IN THE +10V REF WILL CAUSE A GAIN CHANGE IN THE ADC AND THE ZERO CHANGE IN THE S-H.

ANALOG AND DIGITAL GROUNDS ARE CONNECTED TOGETHER IN THE ADC.

WHEN MEASURING VOLTAGES IN THE ADC SYSTEM IT IS RECOMMENDED THAT A RESISTOR BE CONNECTED IN SERIES WITH THE DVM LEAD(S) TO AVOID POSSIBLE OSCILLATIONS THAT MAY BE CREATED IN THE ADC CIRCUITRY DUE TO THE DVM CONNECTION. THIS COULD APPEAR AS AN OFFSET OR UNSTABLE VOLTAGE READING.

AIRFLOW IS CRITICAL TO REPEATABILITY. USE CARE IN MAKING ANY ADJUSTMENTS DONE THRU THE TOP COVER. RECHECK MEASUREMENTS A FEW MINUTES AFTER FIRST MADE. TRY TO MAINTAIN AIRFLOW AS CLOSE AS POSSIBLE TO THE AIRFLOW WITH THE STANDARD COVER INSTALLED.

DON'T EXPECT PERFECT REPEATABILITY. IF LINEARITY IS PLOTTED FOR SEVERAL RUNS IN SUCCESSION SMALL DIFFERENCES CAN USUALLY BE NOTICED. THIS IS PARTLY DUE TO INTERPRETATION OF TRANSITION POINT READINGS, AND IS MUCH MORE NOTICABLE FOR AMP-MUX CHANNELS THAN FET-MUX CHANNELS.

A CHANGE IN THE +10V REF WILL CAUSE A CORRESPONDING CHANGE TO THE -10V REF. THE RESULTING -10V CHANGE WILL NOT AFFECT THE ADC BUT WILL CAUSE A ZERO SHIFT IN THE S-H. THE CHANGE IN THE +10V REF WILL CAUSE A GAIN CHANGE IN THE ADC AND THE ZERO CHANGE IN THE S-H.

ANALOG AND DIGITAL GROUND ARE CONNECTED TOGETHER IN THE ADC.

WHEN MEASURING VOLTAGES IN THE ADC SYSTEM IT IS RECOMMENDED THAT A RESISTOR BE CONNECTED IN SERIES WITH THE DVM LEAD(S) TO AVOID POSSIBLE OSCILLATIONS THAT MAY BE CREATED IN THE ADC CIRCUITRY DUE TO THE DVM CONNECTION. THIS COULD APPEAR AS AN OFFSET OR UNSTABLE VOLTAGE.

AIRFLOW IS CRITICAL TO REPEATABILITY. USE CARE IN MAKING ANY ADJUSTMENTS DONE THRU THE TOP COVER. CHECK MEASUREMENTS A FEW MINUTES AFTER FIRST MADE. TRY TO MAINTAIN AIRFLOW AS CLOSE AS POSSIBLE TO THE AIRFLOW WITH THE STANDARD COVER INSTALLED.

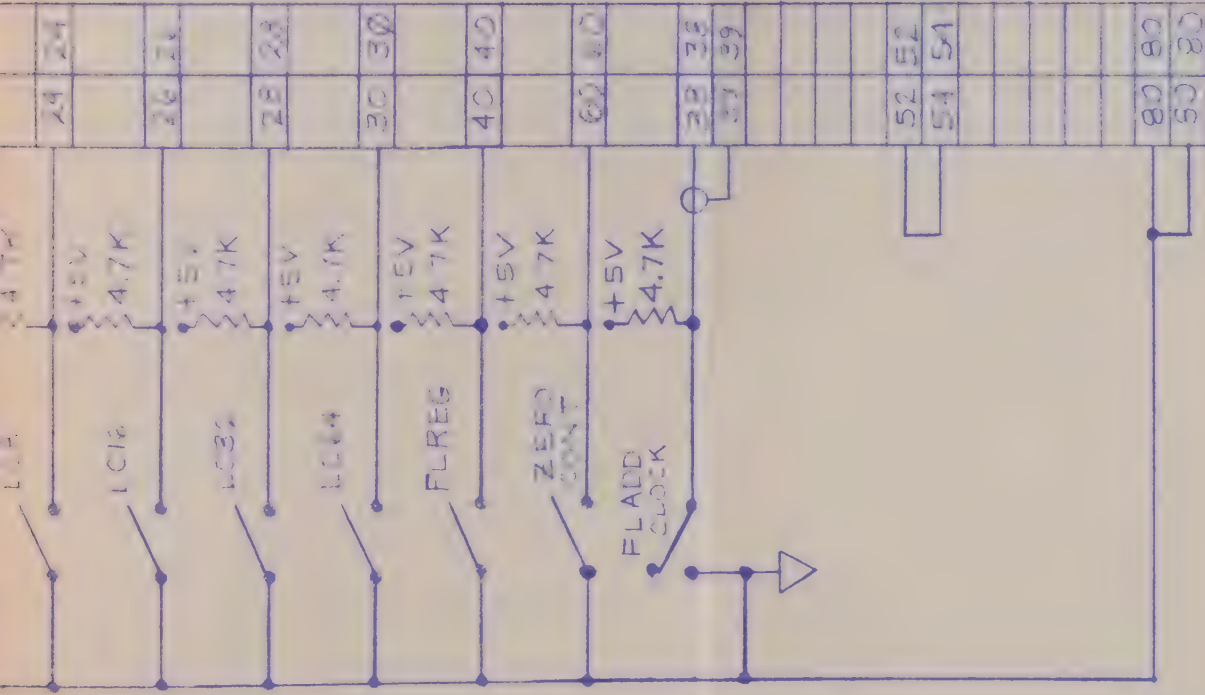
DON'T EXPECT PERFECT REPEATABILITY. IF LINEARITY IS PLOTTED FOR SEVERAL RUNS IN SUCCESSION SMALL DIFFERENCES CAN USUALLY BE NOTICED. THIS IS PARTLY DUE TO INTERPRETATION OF TRANSITION POINT READINGS, AND IS MUCH MORE NOTICEABLE FOR AMP-MUX CHANNELS THAN RET-MUX CHANNELS.

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FIGURE TMX-21	S-H BLOCK DIAGRAM
FIGURE TMX-22	ANALOG INPUT CONNECTIONS 4 SHEETS
FIGURE TMX-23	ADC BLOCK DIAGRAM

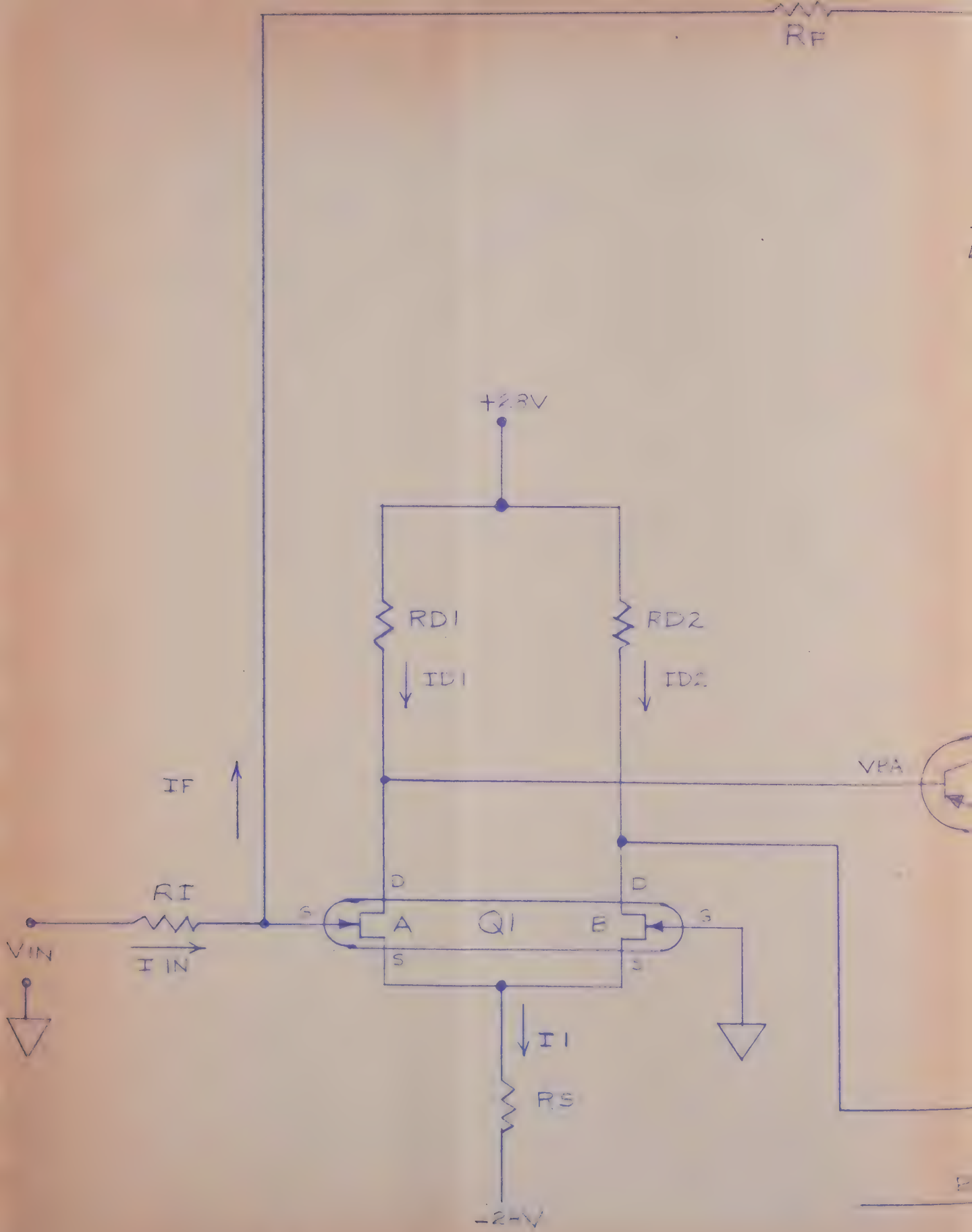
*** LIST OF FIGURES ***

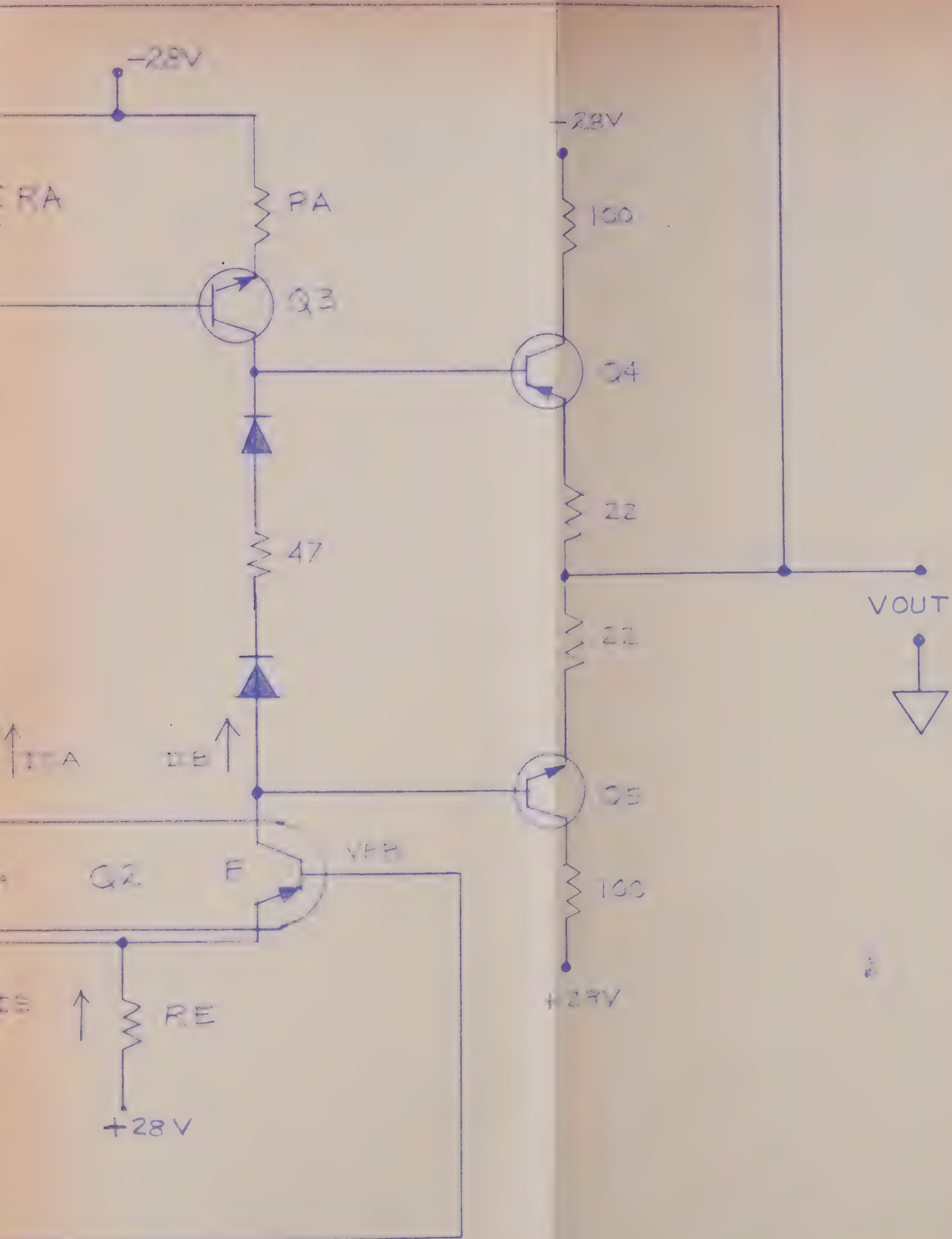
FIGURE 1	EXTERNAL SWITCH CONNECTIONS
FIGURE 2	BASIC OPERATIONAL AMPLIFIER
FIGURE 3	AMP-LOGIC "A" BLOCK DIAGRAM
FIGURE 4	AMP-LOGIC "B" BLOCK DIAGRAM
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FIGURE 22	ANALOG INPUT CONNECTIONS 4 SHEETS
FIGURE 23	ADC BLOCK DIAGRAM



EXTERNAL CONTROLS

FIG TMX-1

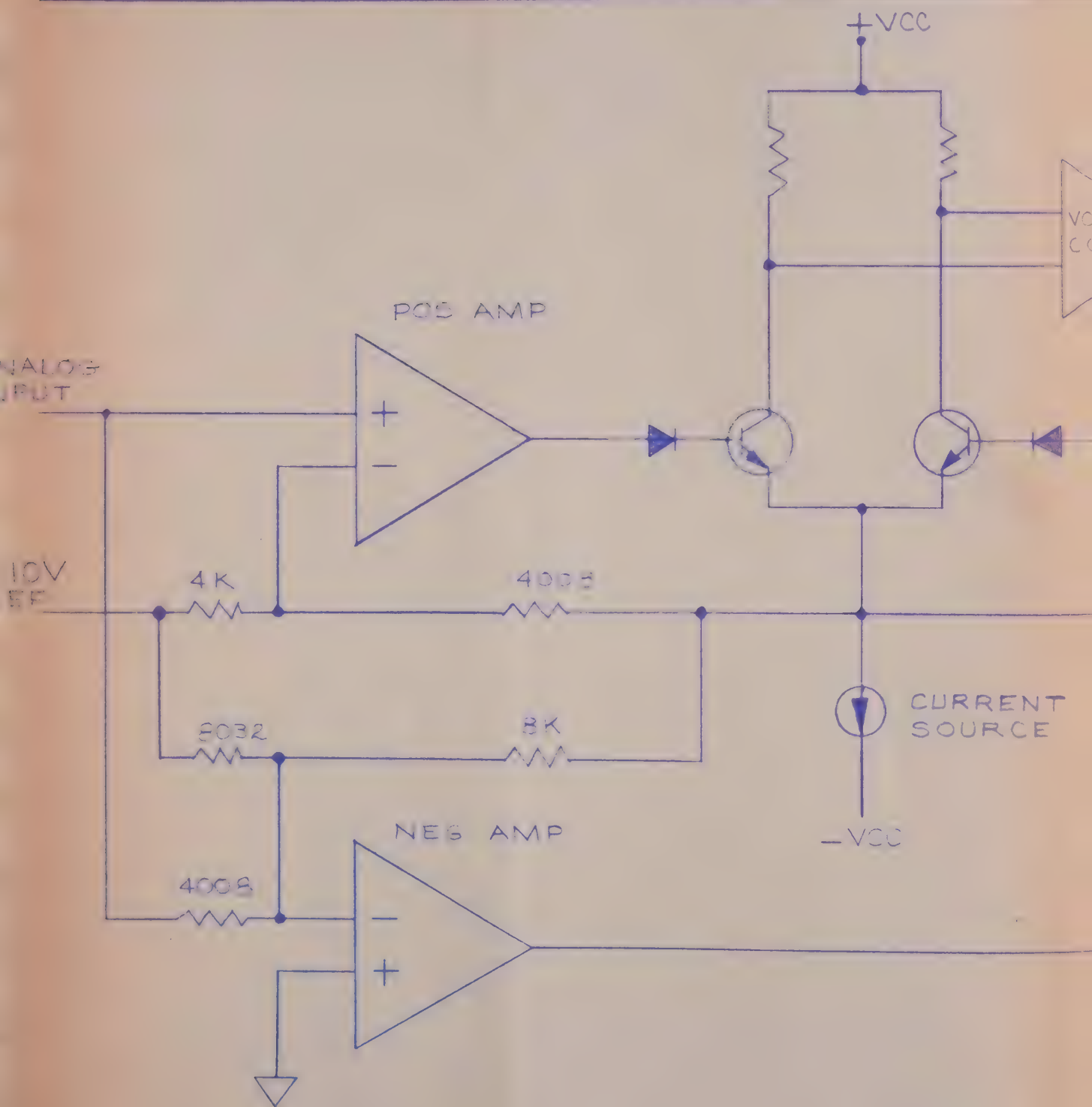


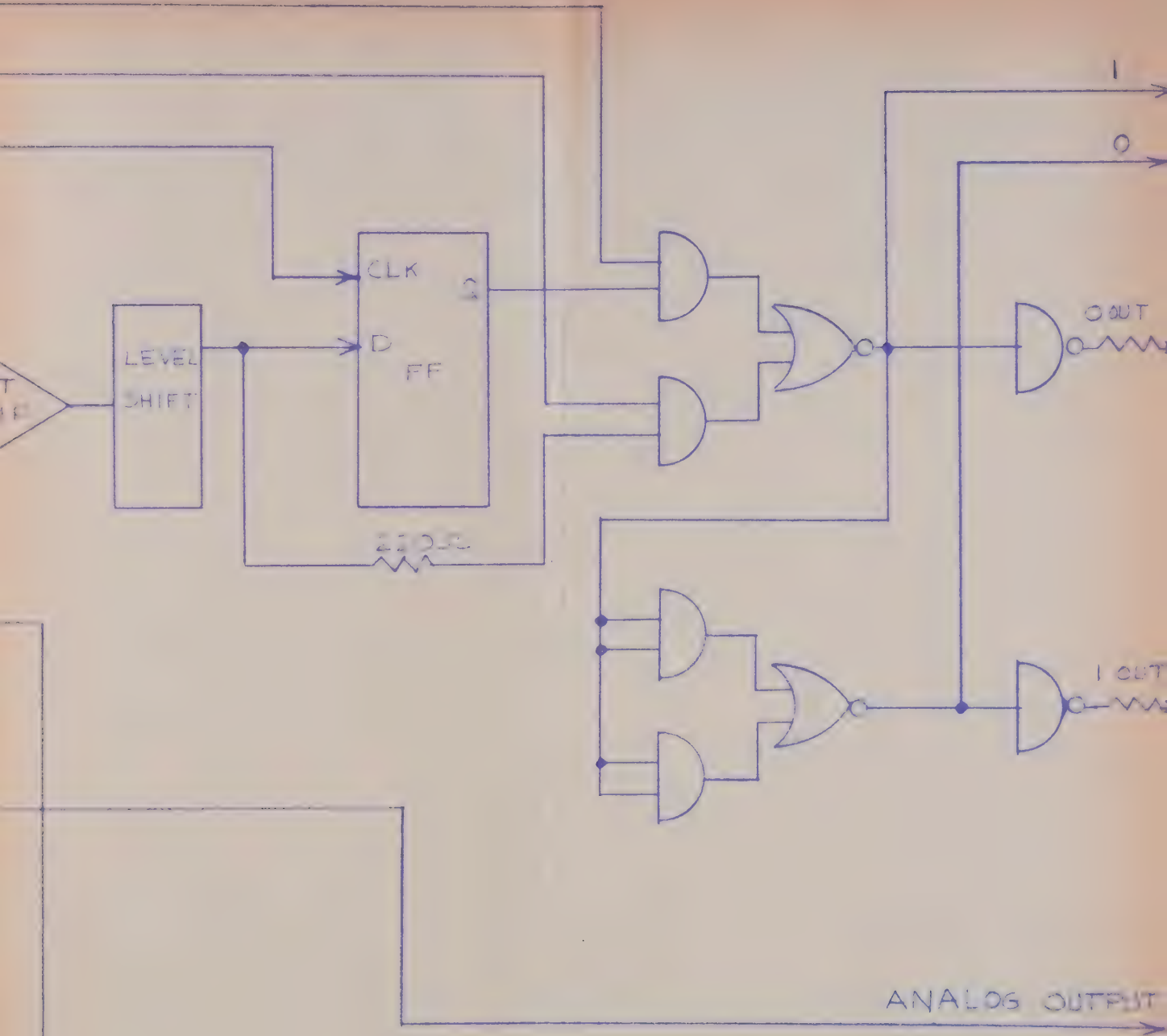


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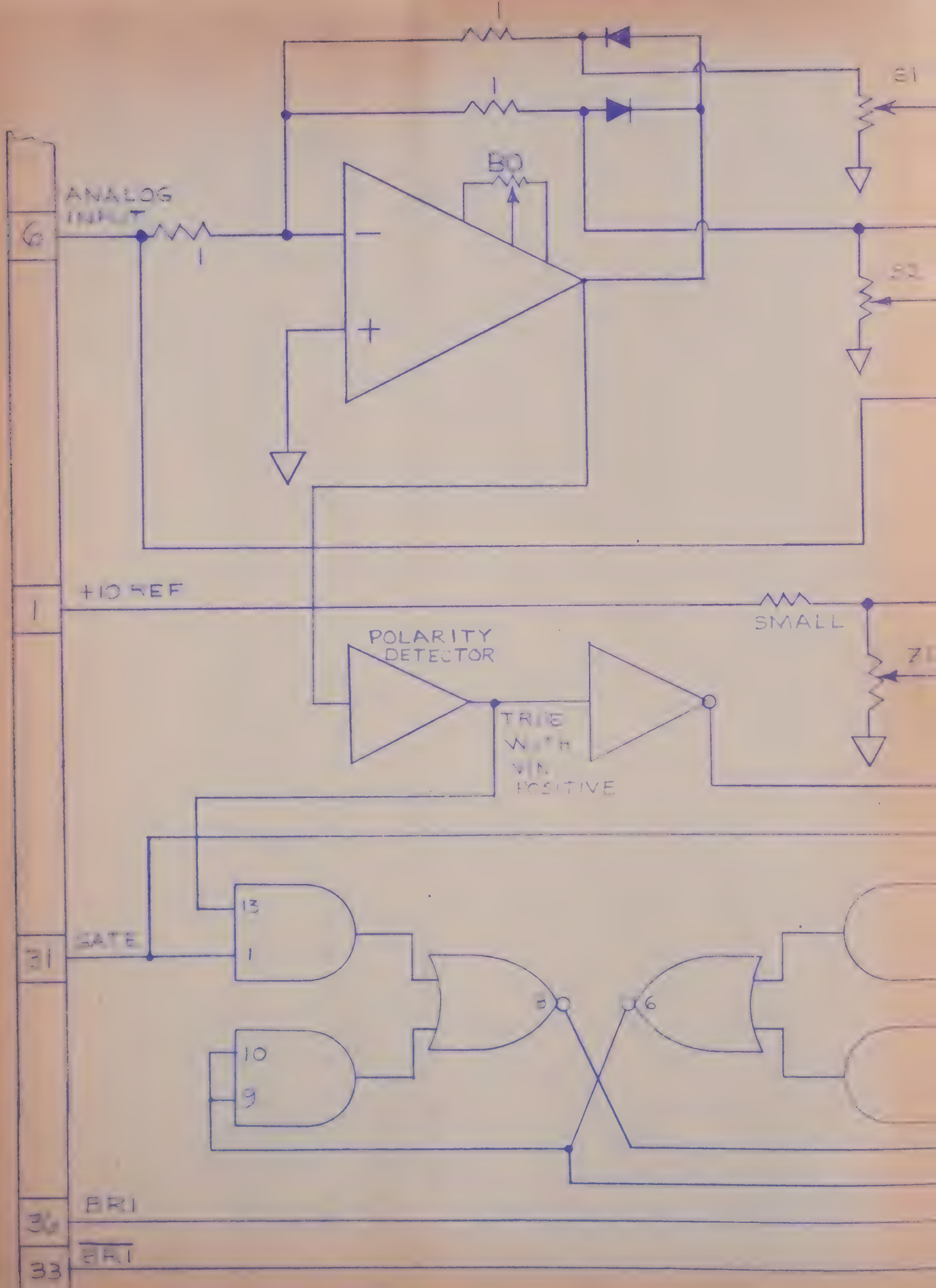
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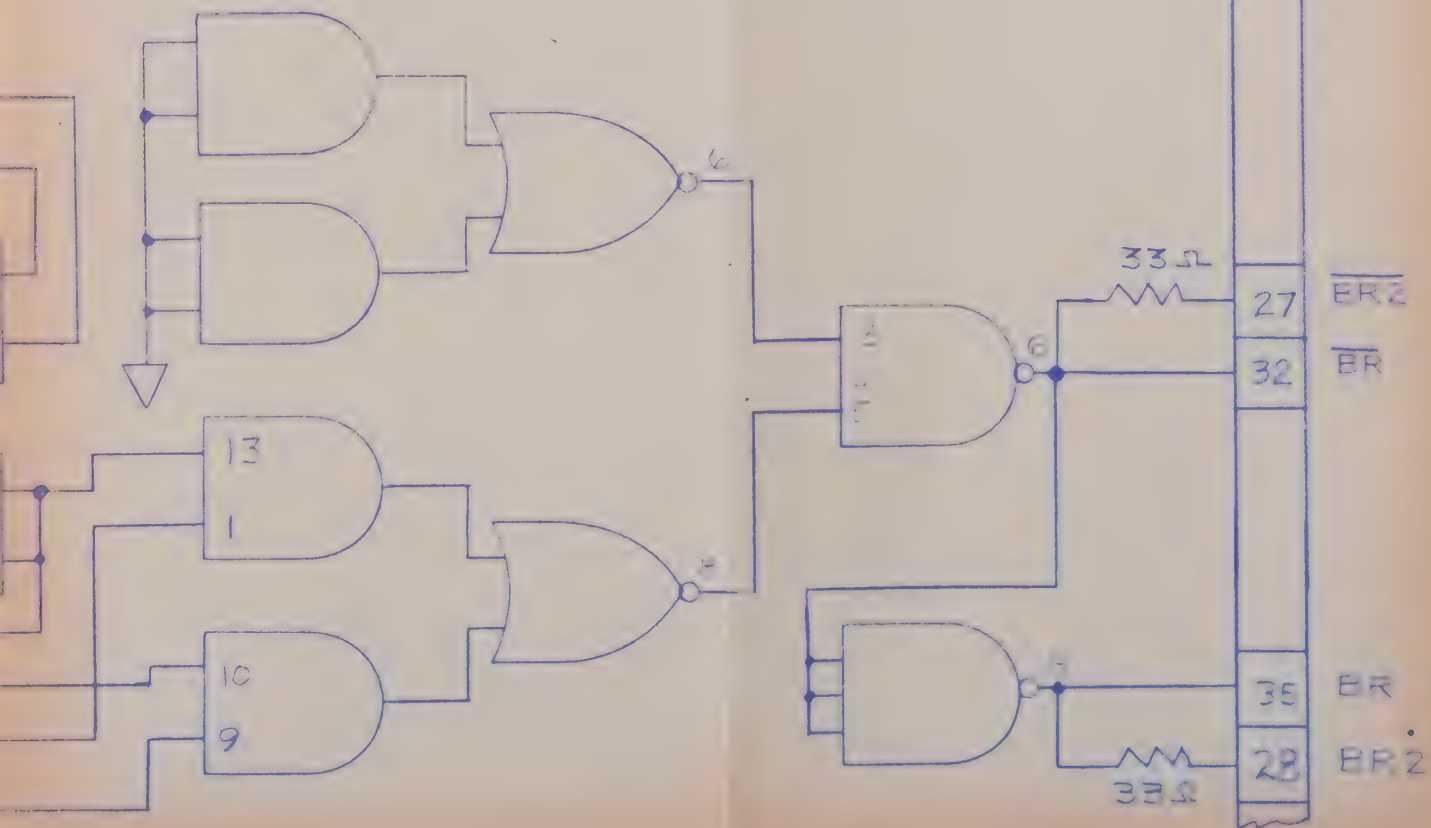
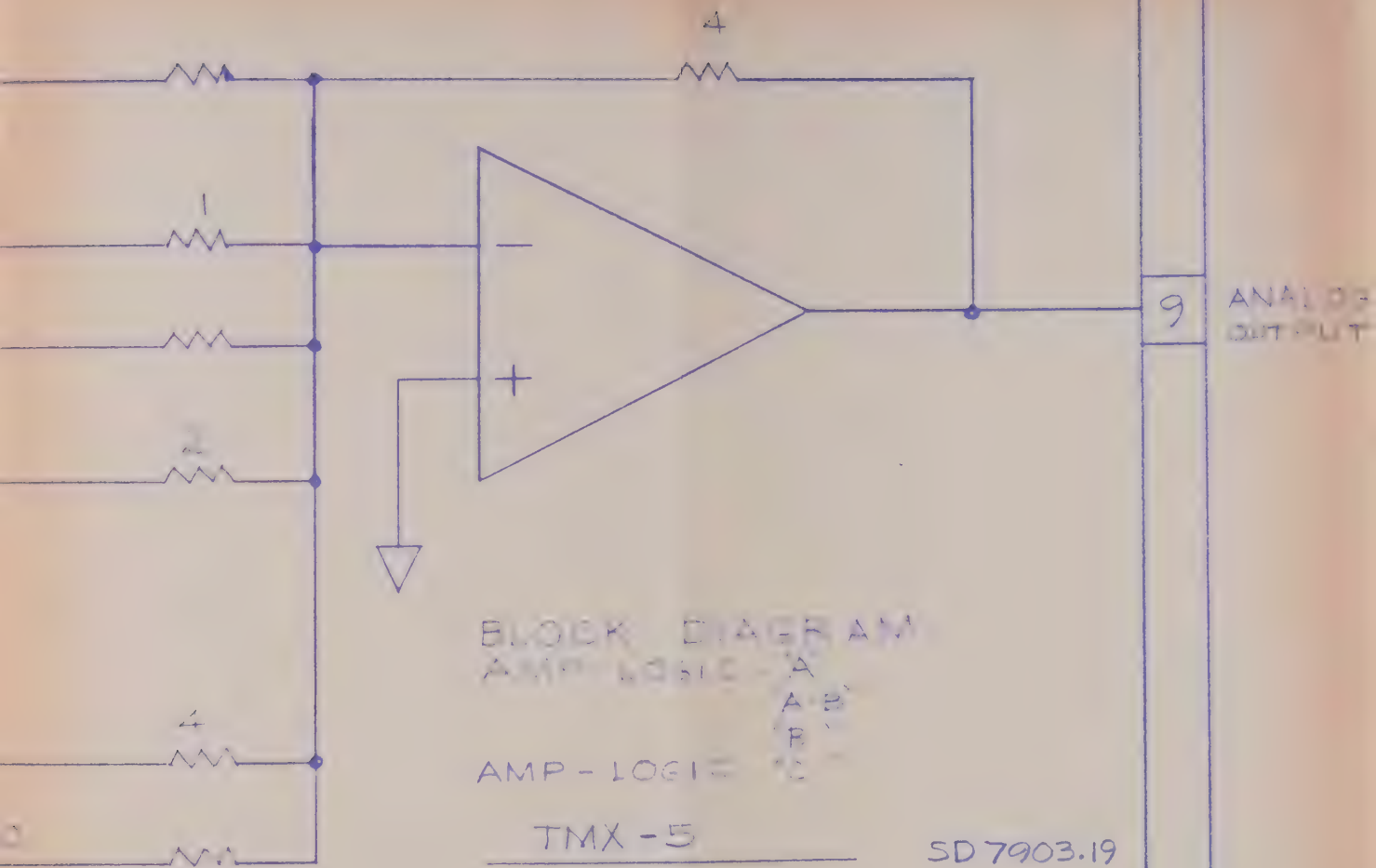
GATE

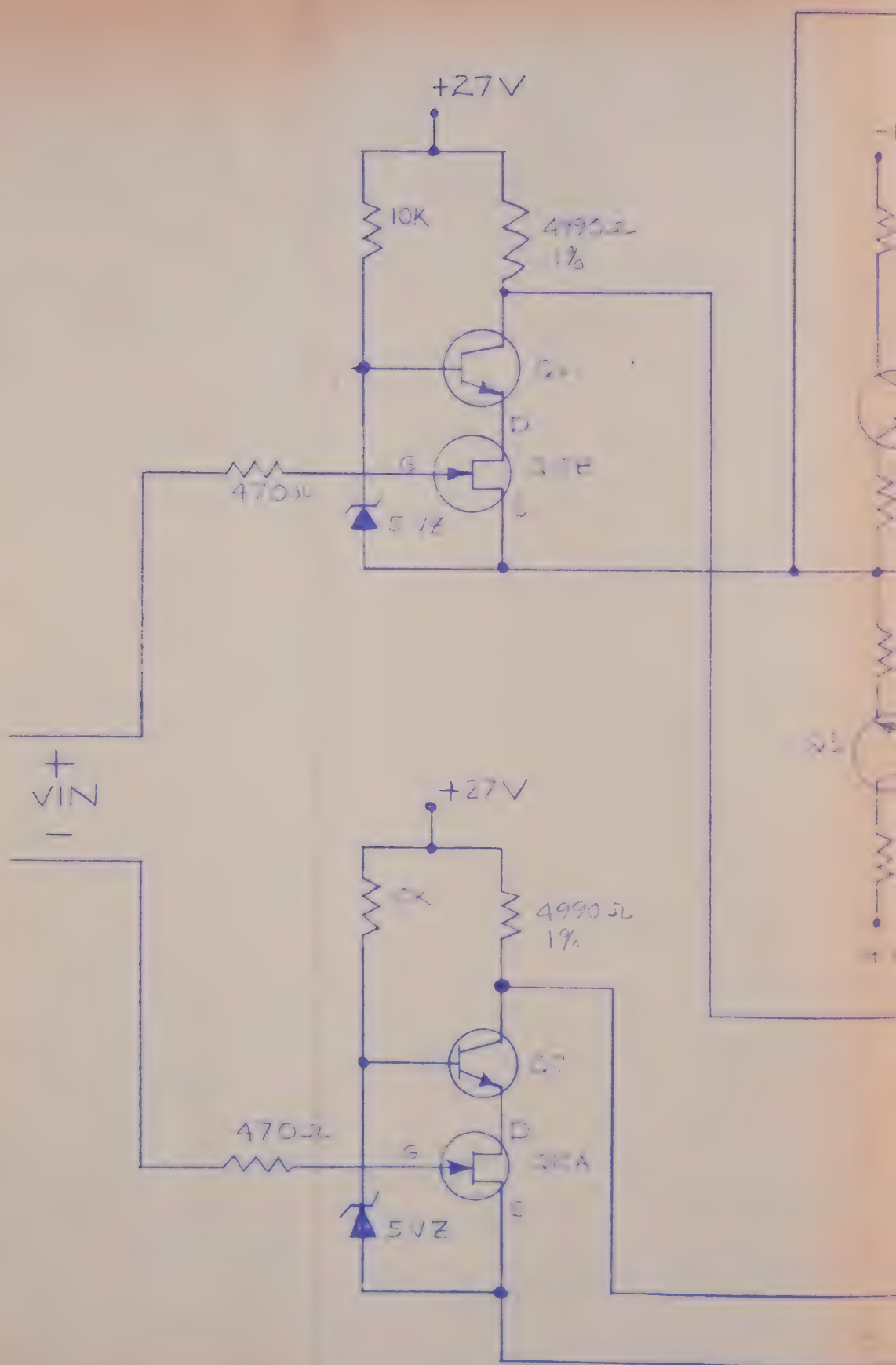




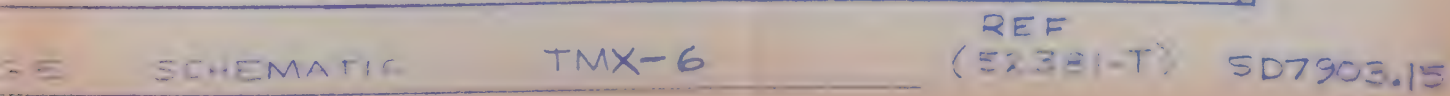
BLOCK DIAGRAM AMP-LOGIC "ZCA" 54275







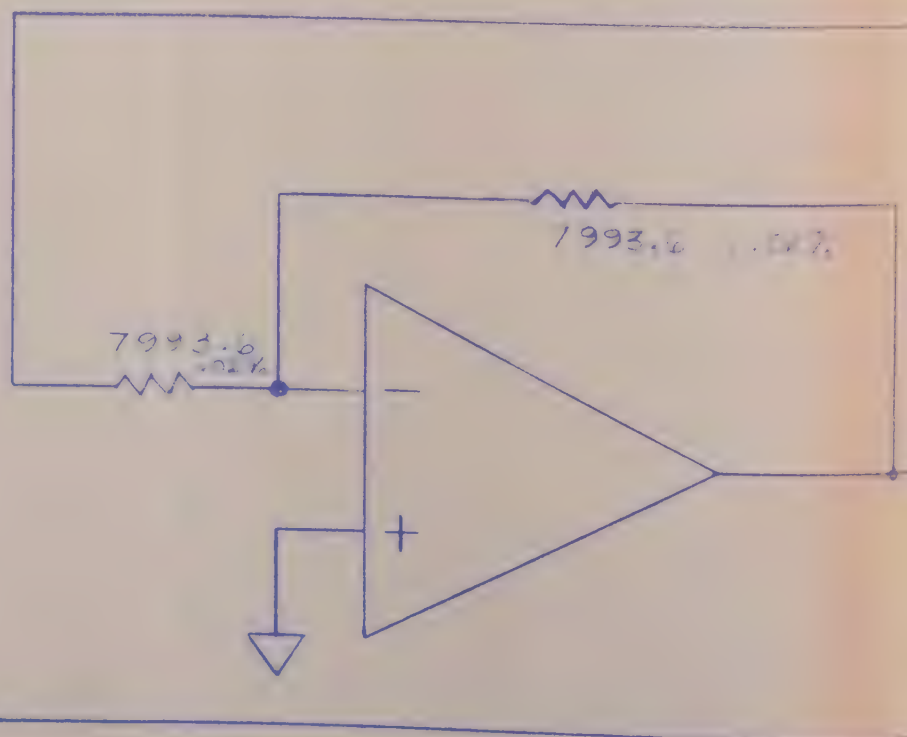
DIFF AMP STAGE

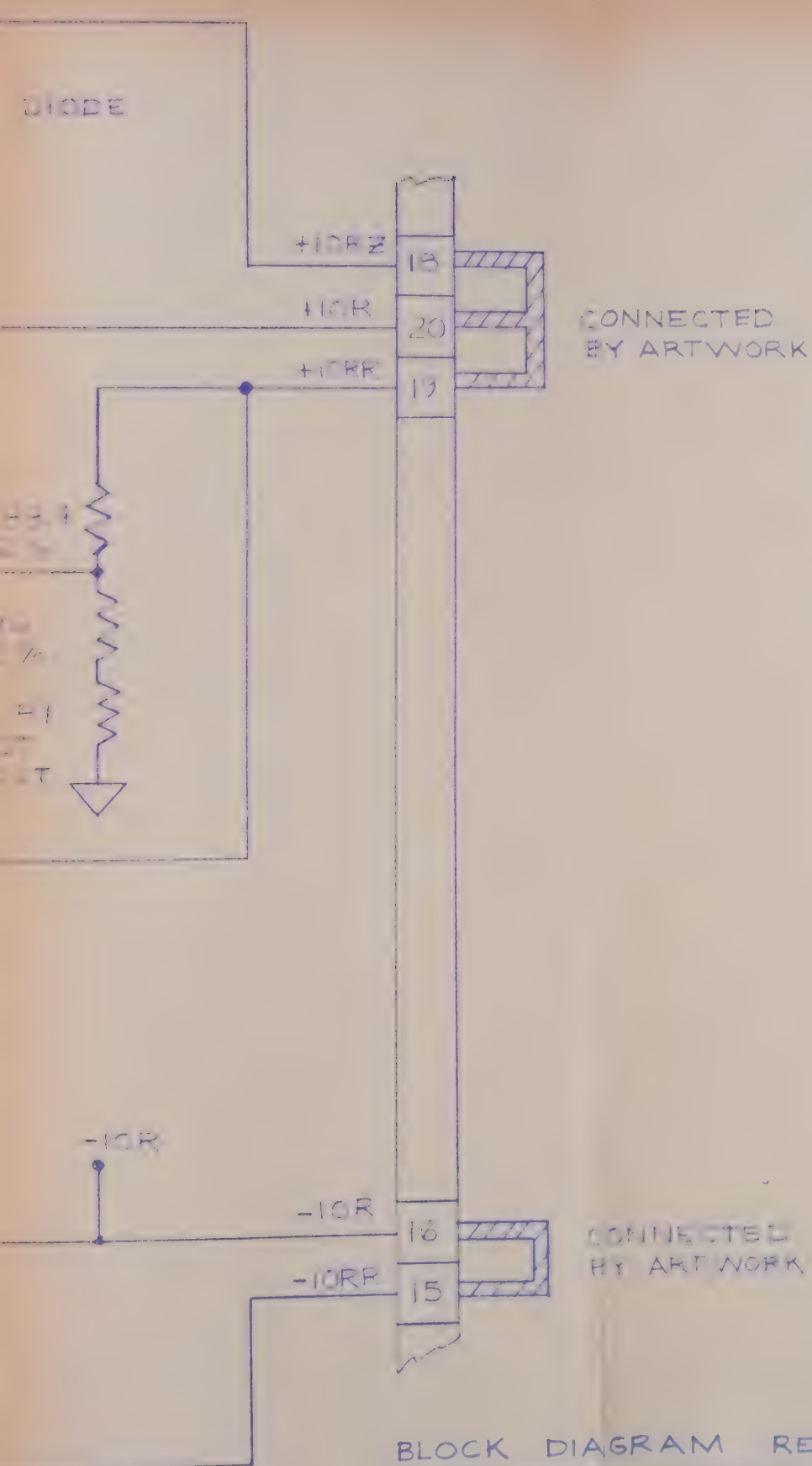


IN825
REFERENC

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+10



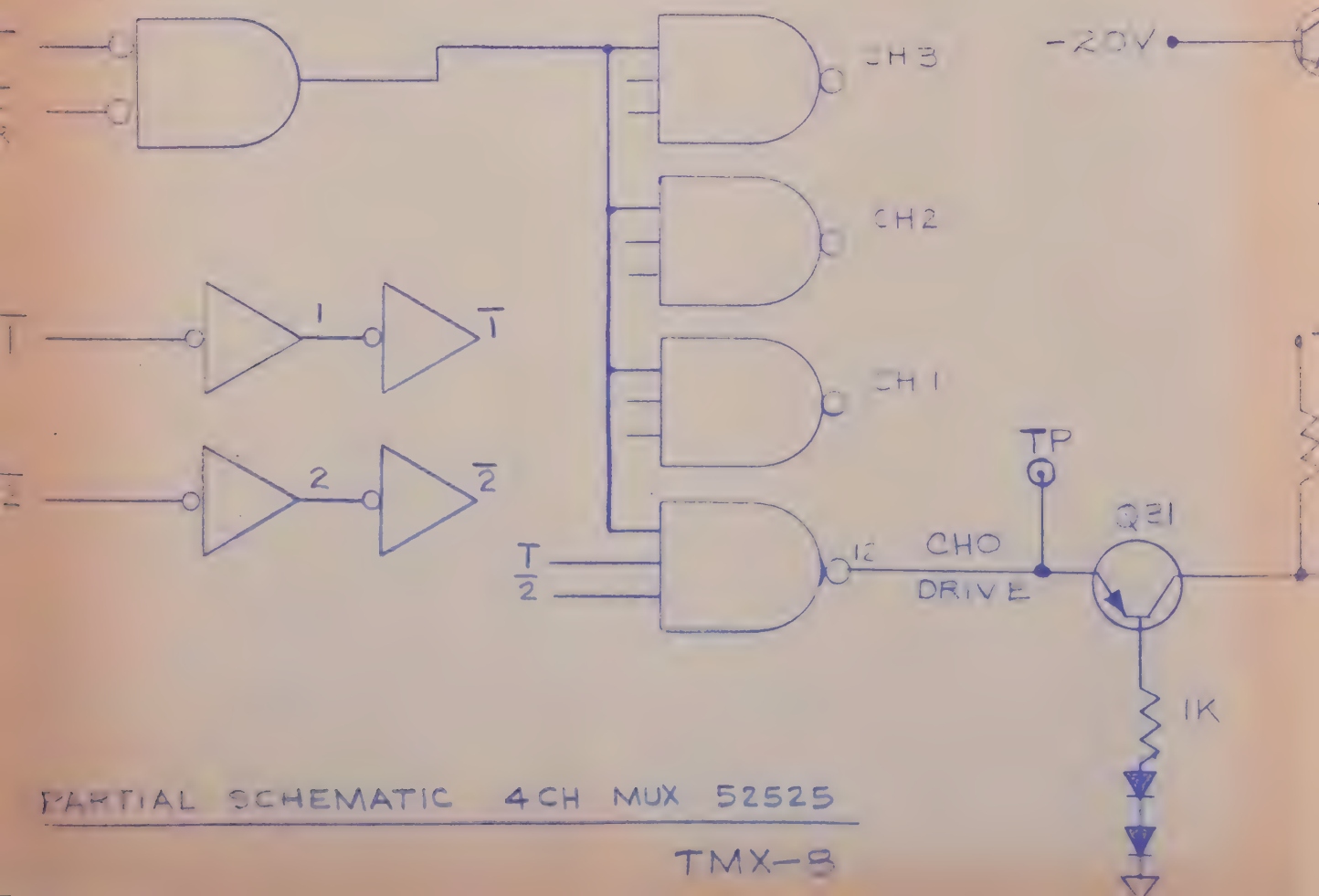
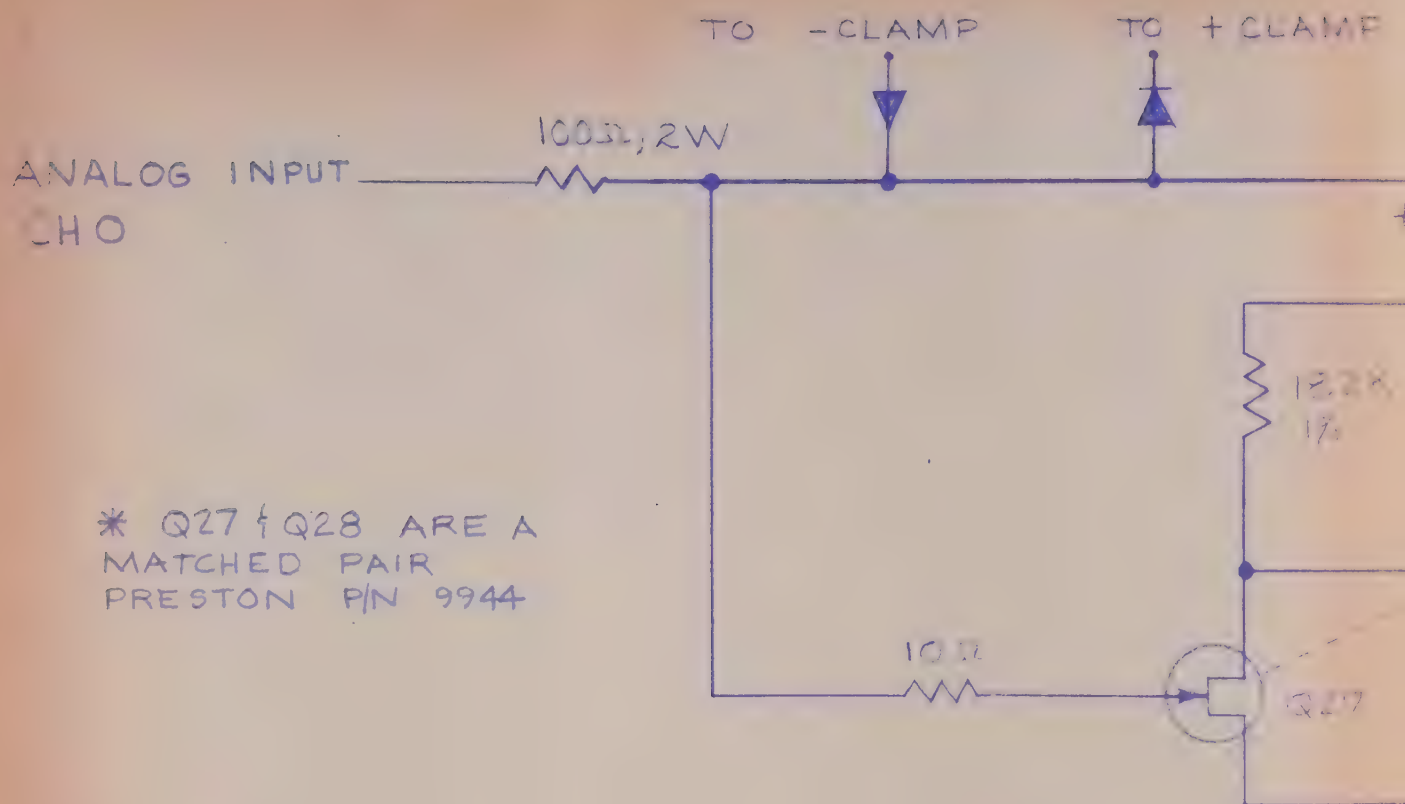


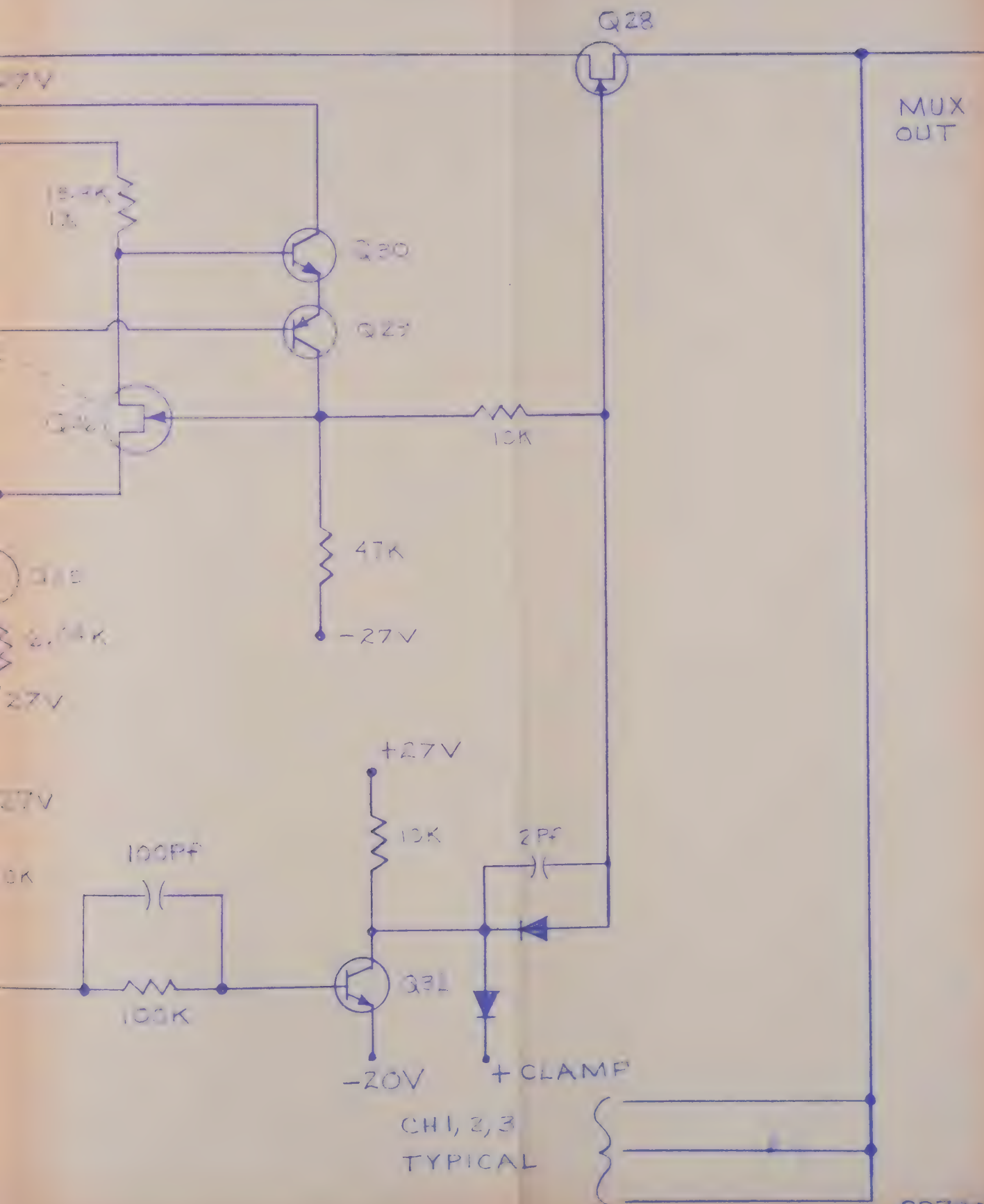
BLOCK DIAGRAM REFERENCE SUPPLIES

59055

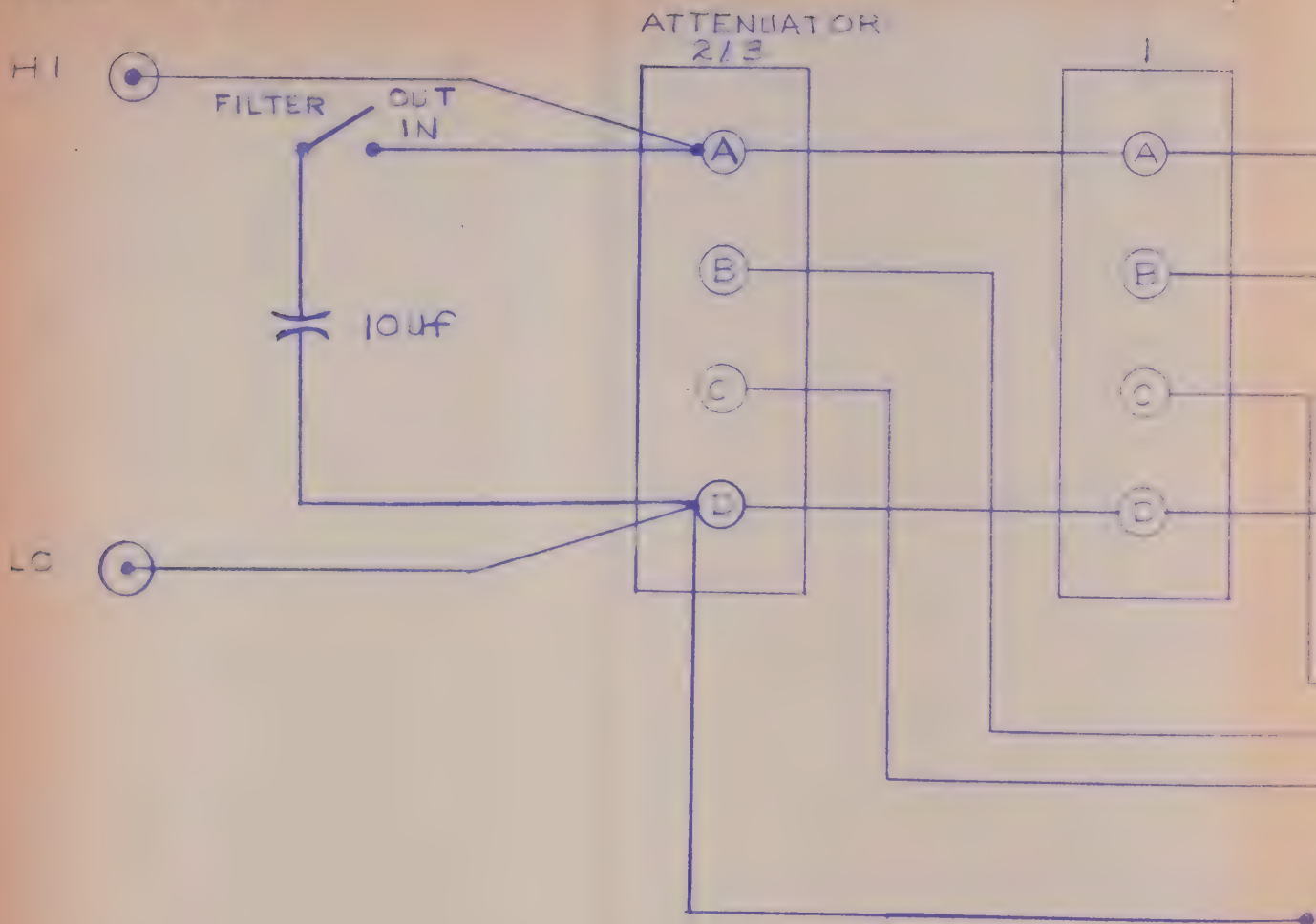
TMX-7

307903.10



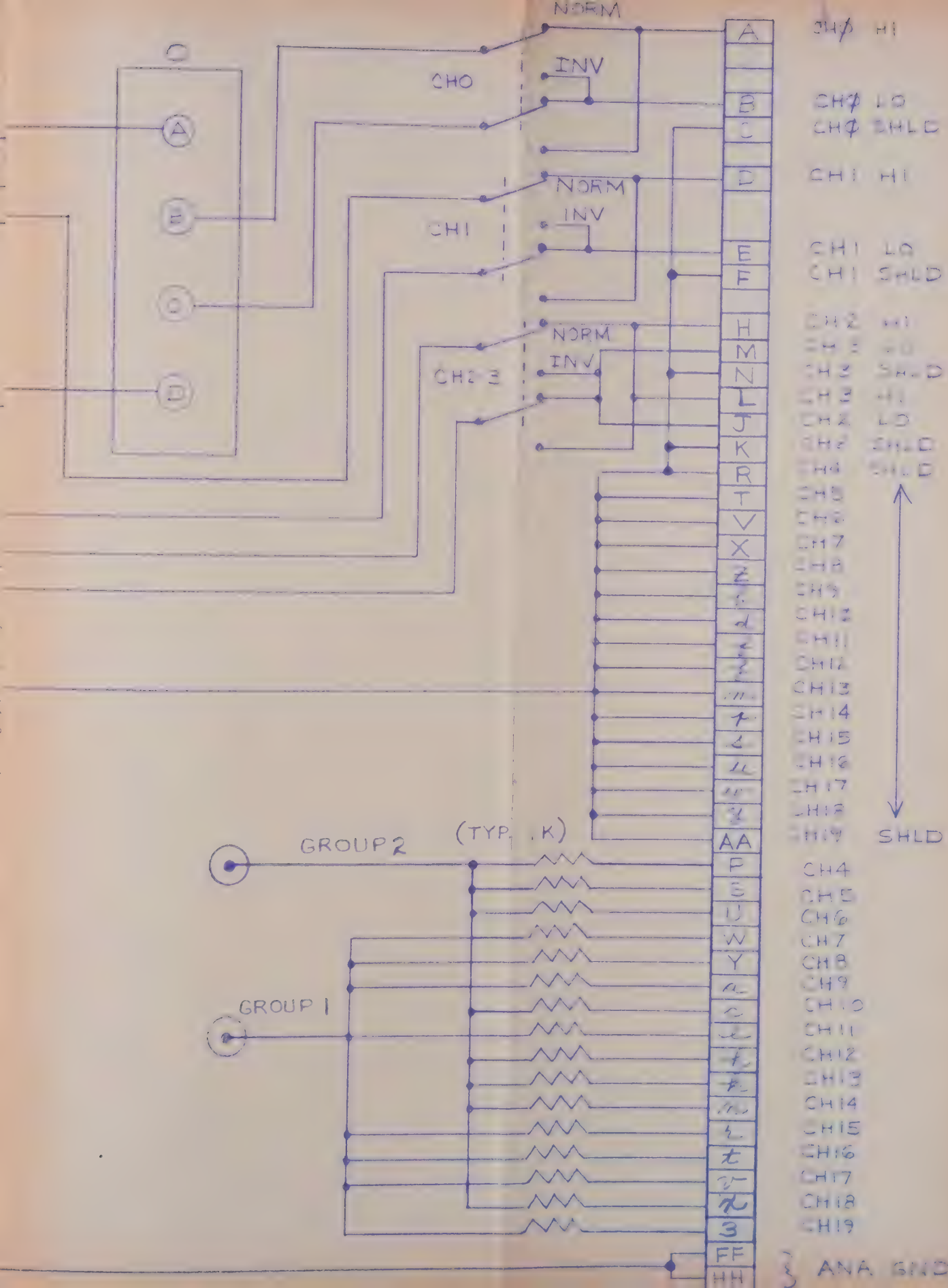


ANALOG INPUT

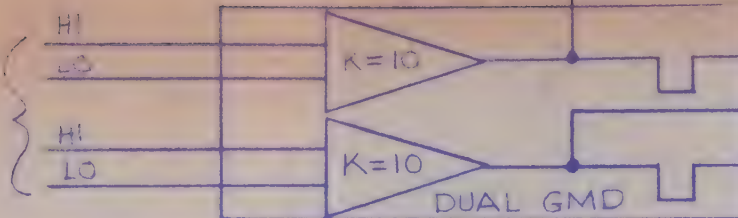


ANALOG INPUTS

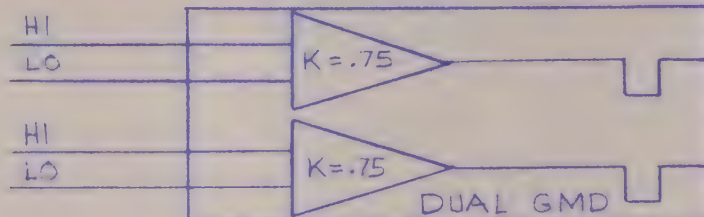
FIGURE TMX-9



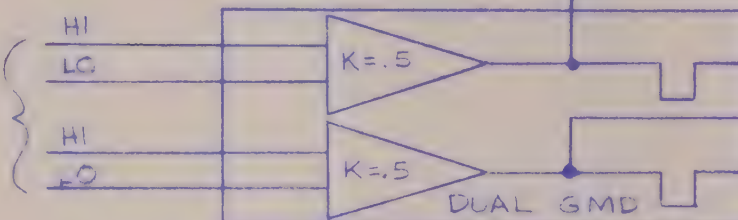
TYP CH20-24
 $\pm 1.024 \text{ VFS}$
 2 CH / CARD



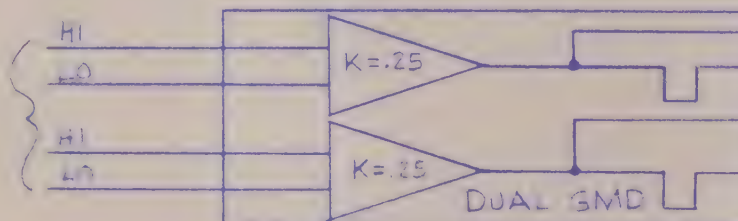
$\pm 13.6533 \text{ VFS}$ CH30



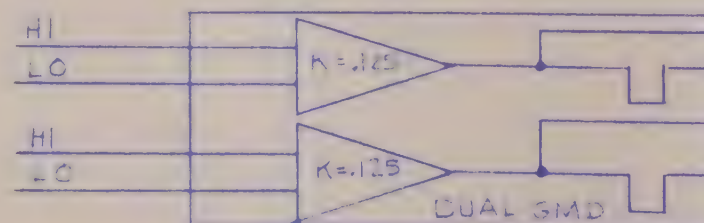
TYP CH32-39
 $\pm 20.48 \text{ VFS}$
 2 CH / CARD



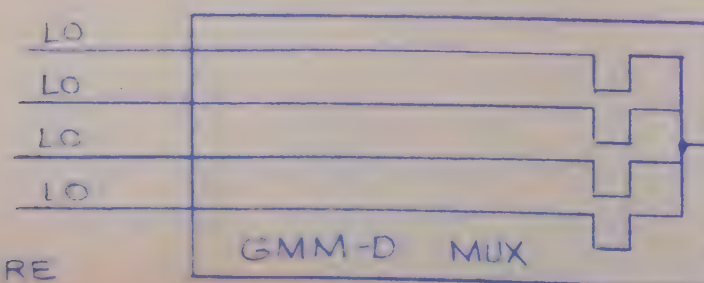
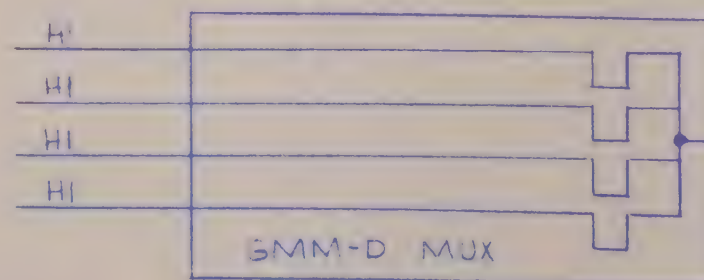
TYP CH40-51
 $\pm 40.96 \text{ VFS}$
 2 CH / CARD



TYP CH52-55
 $\pm 81.92 \text{ VFS}$
 2 CH / CARD



TYP CH 64/103
 $\pm 10.24 \text{ VFS}$
 4 CH / 2 CARDS

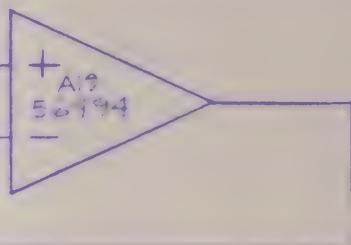


* EXPECTED FUTURE
 ADDITION

CONTINUOUS
ANALOG OUTPUTS
FROM CH SHOWN
ONLY

CH21

C



CH32

E

CH33

H

CH40

K

CH41

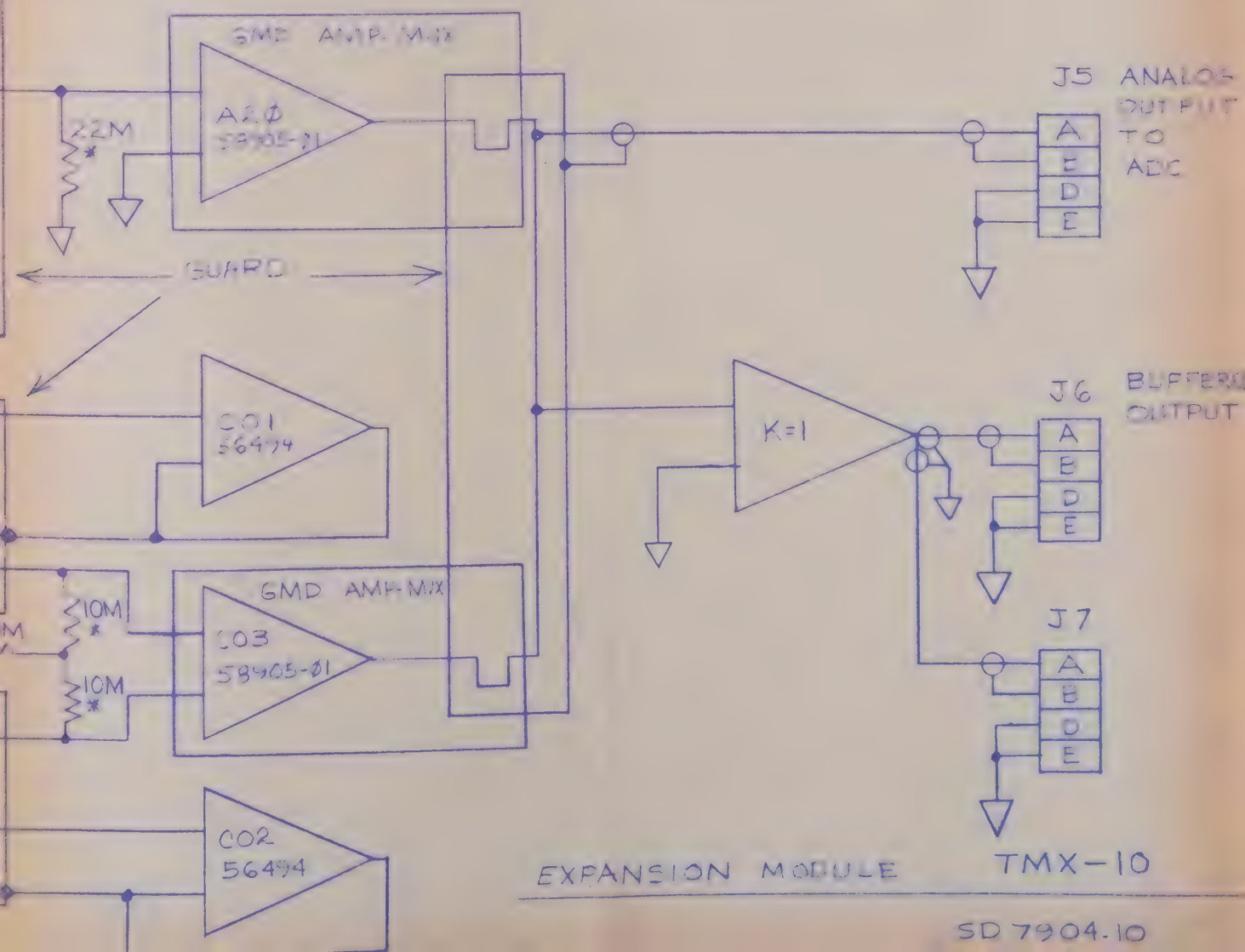
M

CH52

P

CH53

S



A01	± 10V REF SUPPLIES 59655 ALL	C01	GMD AMP-MUX CHO X10 58715-07 53065
A02	SAMPLE-AND-HOLD 52380-14 ALL	C02	GMD AMP-MUX CH1 58715-05 53065-01
A03	ZCA (A1) 54275 -02,03 "A1" 46200 -00,01	C03	GMD AMP-MUX CH2 X1 58720-01
A04	ZERO CROSSING CONT 54283 SIGN STORAGE 58710 -00,01 -02,03	C04	GMD AMP-MUX CH3 X1 58720-01
A05	A2 52640 -02,03 56620 -00,01	C05	4 CH MUX 52525-01 CH4,5,6,7
A06	A3 52640 -02,03 56620 -00,01	C06	4 CH MUX 52525-01 CH8,9,10
A07	A4 52640 -02,03 56620 -00,01	C07	4 CH MUX 52525-01 CH12,13,14,15
A08	A5 52640 -02,03 B1 46016 -00,01	C08	4 CH MUX 52525-01 CH16,17,18,19
A09	A-B 4600 -02,03 B2 46016 -00,01	C09	GUARD DRIVER 56494
A10	B1 46016 ALL	C10	MUX CONTROL STORE 58965
A11	B2 46016 ALL	C11	MUX CONTROL STORE 58965
A12	C1 46023 ALL		
A13	C2 46023 ALL		
A14	C3 46023 ALL		
A15	4 BIT AMP 59520 02,03 46125 00,01		
A16	4 BIT LOGIC 46175 ALL		
A17	ADC CONTROL 52535-02 ALL		
A18	MUX DECODE 52545 ALL		
A19	MUX CONTROL 59005 ALL		
A20	MUX COUNTER REGISTER 52530 ALL		

FRONT

POWER SUPPLY

4 DIFF
CHANNELS

SINGLE
ENDED

58700 PLUG-IN BOARD LOCATIONS
TOP VIEW

* THESE CARDS WERE NOT
INSTALLED IN -00 UNITS
AT TIME OF DELIVERY BUT
HAVE SINCE BEEN ADDED.

TMX-11

SD7903.23

LDA 1-10				TYP 10-20			
A01	CH20	56855-05 $\pm 1.024VFS$	CH21	B01	CH 64	65	66
A02	CH22	56855-05 $\pm 1.024VFS$	CH23	B02	CH 64	65	66
A03	CH24	56855-05 $\pm 1.024VFS$	CH25	B03	CH 68	69	70
A04	CH26	56855-05 $\pm 1.024VFS$	CH27	B04	CH 68	69	70
A05	CH28	56855-05 $\pm 1.024VFS$	CH29	B05	CH 72	73	74
A06	CH30	56855-05 $\pm 1.024VFS$	CH31	B06	CH 72	73	74
A07	CH32	56855-06 $\pm 20.48VFS$	CH33	B07	CH 76	77	78
A08	CH34	56855-06 $\pm 20.48VFS$	CH35	B08	CH 76	77	78
A09	CH36	56855-06 $\pm 20.48VFS$	CH37	B09	CH 80	81	82
A10	CH38	56855-06 $\pm 20.48VFS$	CH39	B10	CH 80	81	82
A11	CH40	56855-07 $\pm 40.96VFS$	CH41	B11	CH 84	85	86
A12	CH42	56855-07 $\pm 40.96VFS$	CH43	B12	CH 84	85	86
A13	CH44	56855-07 $\pm 40.96VFS$	CH45	B13	CH 88	89	90
A14	CH46	56855-07 $\pm 40.96VFS$	CH47	B14	CH 88	89	90
A15	CH48	56855-07 $\pm 40.96VFS$	CH49	B15	CH 92	93	94
A16	CH50	56855-07 $\pm 40.96VFS$	CH51	B16	CH 92	93	94
A17	CH52	56855-08 $\pm 81.92VFS$	CH53	B17	CH 96	97	98
A18	CH54	56855-08 $\pm 81.92VFS$	CH55	B18	CH 96	97	98
A19	GUARD DRIVER CH56			B19	CH 100	101	102
A20	GMD SUB-MUX 58905-01			B20	CH 100	101	102

- C01 GUARD DRIVER 56494
- C02 GUARD DRIVER 56494
- C03 EMD SUB MIX 58903-01
- C04 OUTPUT BUFFER AMP
56445-15
- C05
- C06 LOGIC BUFFER 58445
- C07
- C08 LOGIC BUFFER 40120-15
- C09

POWER SUPPLY

58845
PAUG-IN BOARD
LOCATIONS

TMX-12

FIGURE TMX-13

ANALOG INPUT = +/- 10.2400 VFS:

RESOLUTION = 14 BITS AND SIGN

*** INDICATES 100 / 011

TRANSITION

TWO'S COMPLEMENT NUMBER

THEORETICAL INPUT

ACTUAL INPUT

1 0 0 0 0 0 0 0 0 0 0 1 0 ***	- 10.2278 VOLTS	_____
1 0 0 0 1 1 1 1 1 1 1 0 ***	- 8.9678 VOLTS	_____
1 0 0 1 0 0 0 0 0 0 1 0 ***	- 8.9478 VOLTS	_____
1 0 0 1 1 1 1 1 1 1 1 0 ***	- 7.6878 VOLTS	_____
1 0 1 0 0 0 0 0 0 0 1 0 ***	- 7.6678 VOLTS	_____
1 0 1 0 1 1 1 1 1 1 1 0 ***	- 6.4178 VOLTS	_____
1 0 1 1 0 0 0 0 0 0 1 0 ***	- 6.3878 VOLTS	_____
1 0 1 1 1 1 1 1 1 1 1 0 ***	- 5.1278 VOLTS	_____
1 1 0 0 0 0 0 0 0 0 1 0 ***	- 5.1078 VOLTS	_____
1 1 0 0 1 1 1 1 1 1 1 0 ***	- 3.8478 VOLTS	_____
1 1 0 1 0 0 0 0 0 0 1 0 ***	- 3.8278 VOLTS	_____
1 1 0 1 1 1 1 1 1 1 1 0 ***	- 2.5678 VOLTS	_____
1 1 1 0 0 0 0 0 0 0 1 0 ***	- 2.5478 VOLTS	_____
1 1 1 0 1 1 1 1 1 1 1 0 ***	- 1.2878 VOLTS	_____
1 1 1 1 0 0 0 0 0 0 1 0 ***	- 1.2678 VOLTS	_____
1 1 1 1 1 1 1 1 1 1 1 0 ***	- 0.0078 VOLTS	_____
0 0 0 0 0 0 0 0 0 0 1 0 ***	+ 0.0122 VOLTS	_____
0 0 0 0 1 1 1 1 1 1 1 0 ***	+ 1.2722 VOLTS	_____
0 0 0 1 0 0 0 0 0 0 1 0 ***	+ 1.2922 VOLTS	_____
0 0 0 1 1 1 1 1 1 1 1 0 ***	+ 2.5522 VOLTS	_____
0 0 1 0 0 0 0 0 0 0 1 0 ***	+ 2.5722 VOLTS	_____
0 0 1 0 1 1 1 1 1 1 1 0 ***	+ 3.8322 VOLTS	_____
0 0 1 1 0 0 0 0 0 0 1 0 ***	+ 3.8522 VOLTS	_____
0 0 1 1 1 1 1 1 1 1 1 0 ***	+ 5.1122 VOLTS	_____
0 1 0 0 0 0 0 0 0 0 1 0 ***	+ 5.1322 VOLTS	_____
0 1 0 0 1 1 1 1 1 1 1 0 ***	+ 6.3922 VOLTS	_____
0 1 0 1 0 0 0 0 0 0 1 0 ***	+ 6.4122 VOLTS	_____
0 1 0 1 1 1 1 1 1 1 1 0 ***	+ 7.6722 VOLTS	_____
0 1 1 0 0 0 0 0 0 0 1 0 ***	+ 7.6922 VOLTS	_____
0 1 1 0 1 1 1 1 1 1 1 0 ***	+ 8.9522 VOLTS	_____
0 1 1 1 0 0 0 0 0 0 1 0 ***	+ 8.9722 VOLTS	_____
0 1 1 1 1 1 1 1 1 1 1 0 ***	+ 10.2322 VOLTS	_____

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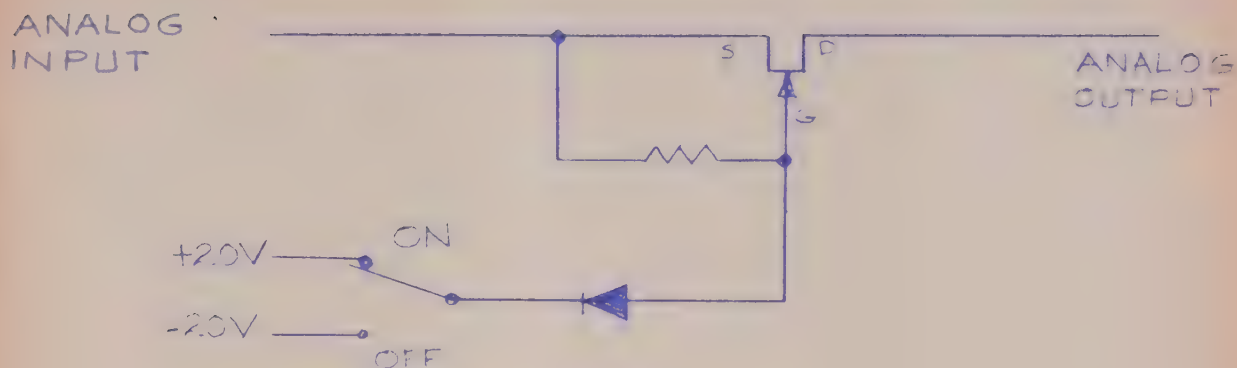
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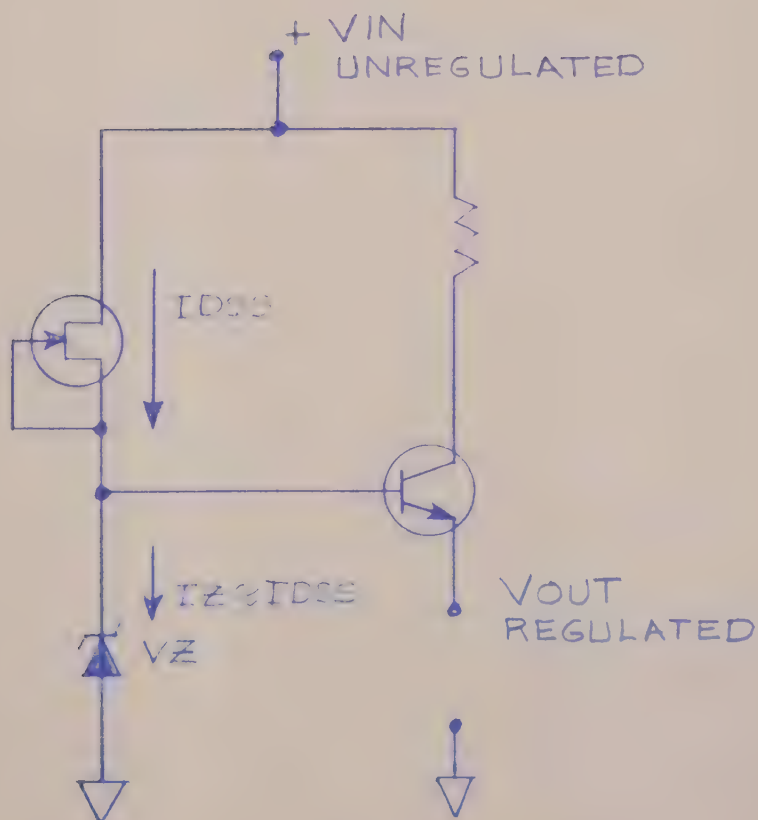
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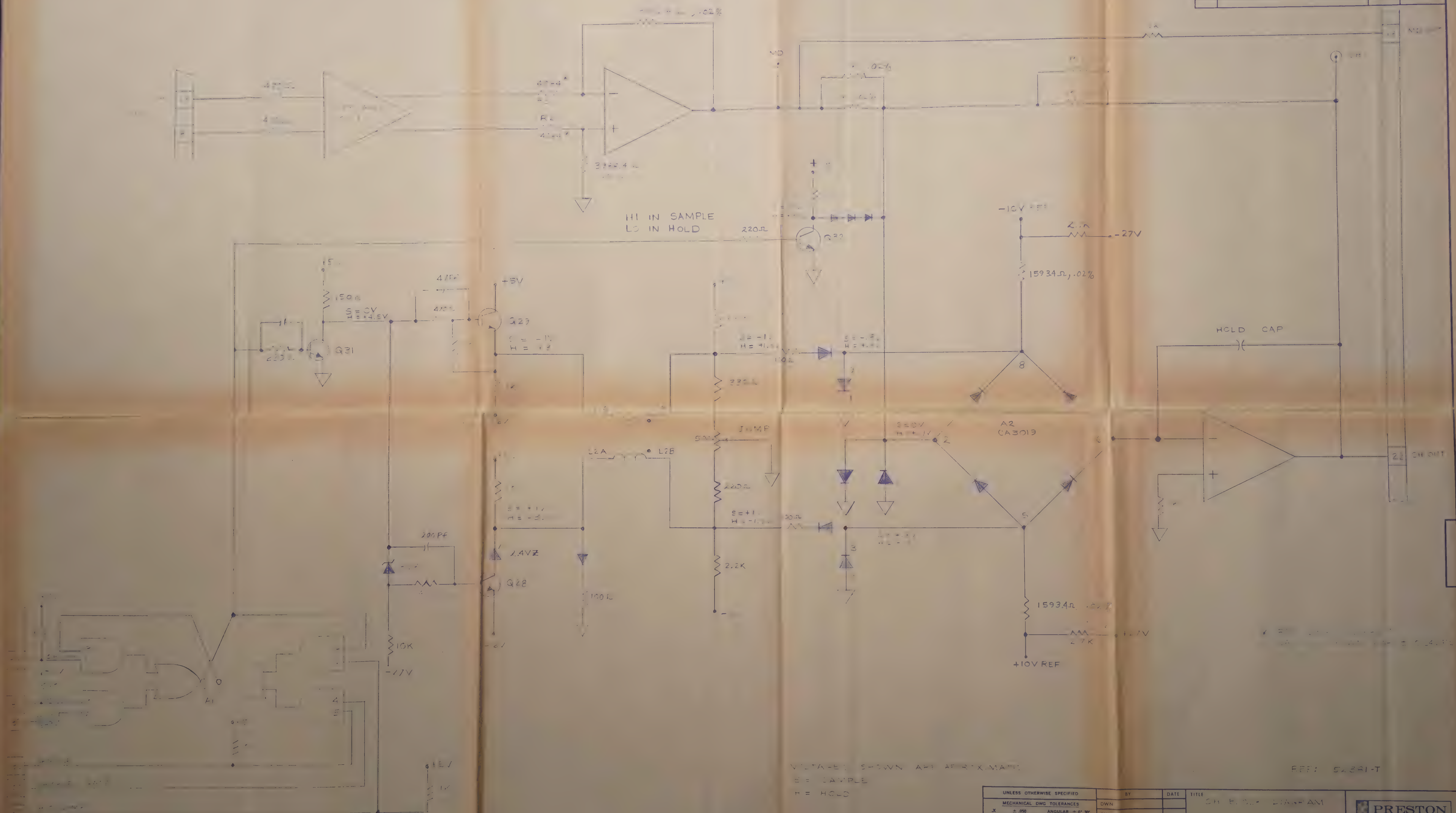


FET SWITCH
FIG TMX-14



FET AS CONSTANT CURRENT SOURCE
FIG TMX-15

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



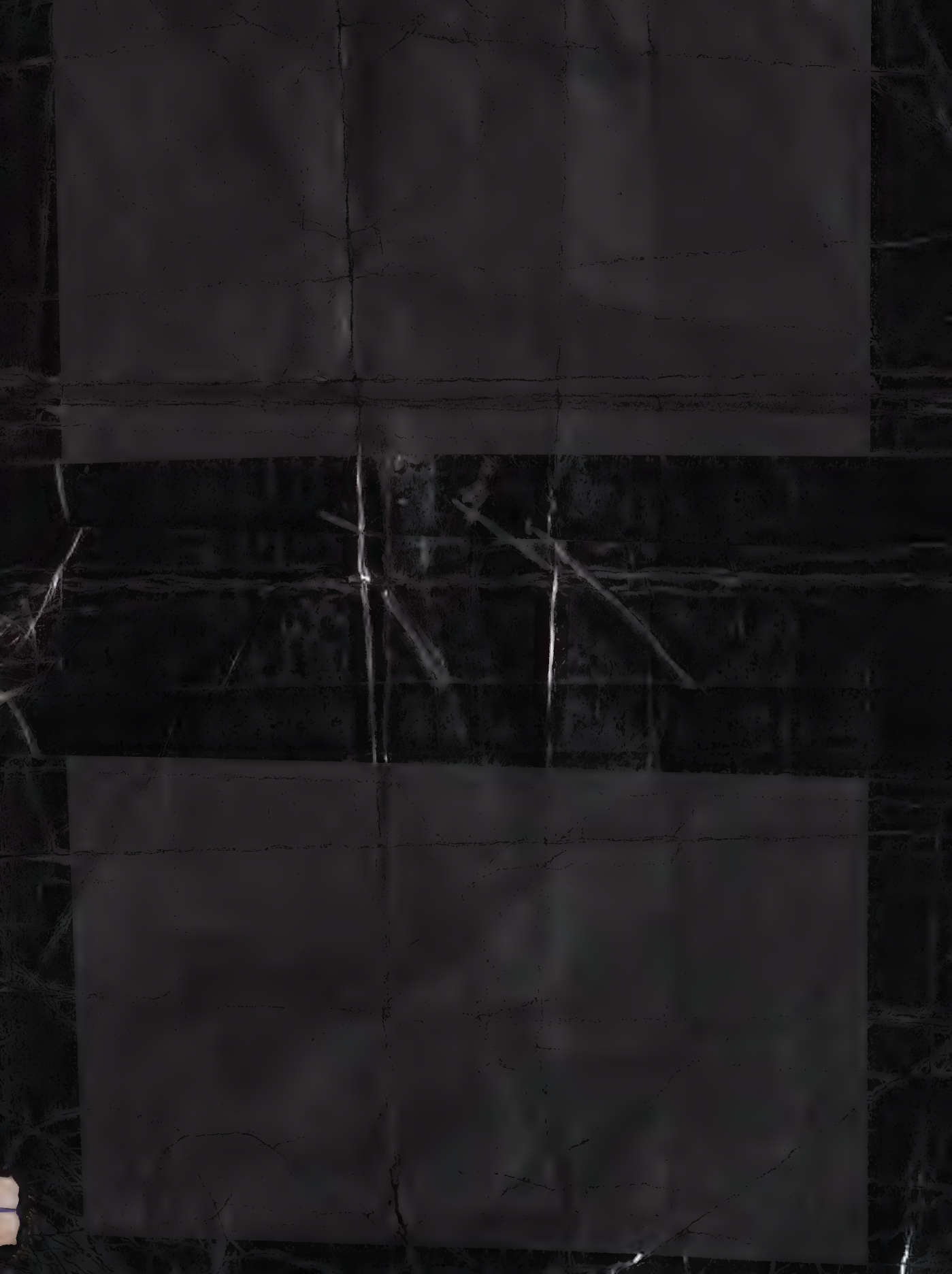
VOLTAGES SHOWN ARE APPROXIMATE
 S = SAMPLE
 H = HOLD

REF: 52381-T

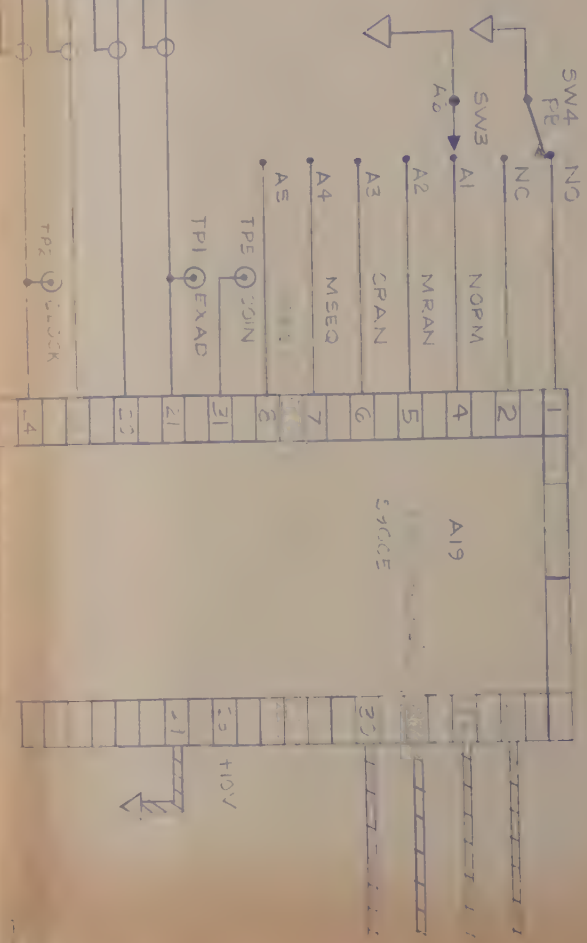
UNLESS OTHERWISE SPECIFIED		BY	DATE	TITLE
MECHANICAL DWG TOLERANCES		DWN		CH BLOCK DIAGRAM
X	± .050	CHK		
XX	± .020	ENG		
XXX	± .005	APP		
THREADS: CLASS 2A OR 2B				
REMOVE BURRS & SHARP EDGES .020 MAX.				
MACH. FILLET RADIUS .020 R MAX.				
MACH. SURF. FLAT WITHIN .001 IN/IN				
OTHER SURF. FLAT WITHIN .005 IN/IN				
ELECTRICAL DWG DESIGNATIONS				
REFERENCE DESIGNATIONS ARE				
ABBREVIATED. PREFIX THE				
DESIGNATION WITH UNIT				
NUMBER OR ASSEMBLY DESIG-				
NATION OR BOTH.				
		NEXT ASSY		
SIZE	SCALE	SH	OF	

PRESTON
 SCIENTIFIC INCORPORATED
 11111 11111 11111 11111 11111
 11111 11111 11111 11111 11111
 11111 11111 11111 11111 11111

D TMX-17



REVISONS		
SYM	DESCRIPTION	DATE



UNLESS OTHERWISE SPECIFIED		BY	DATE	TITLE	 PRESTON INCORPORATED 10000 1st Avenue, Suite 200 San Diego, CA 92121
MECHANICAL DWG TOLERANCES		DWN		INTERCONNECT	
X ± .050 ANGULAR ± 0° 30' XX ± .020 XXX ± .010 MACH. SURF. THREADS, CLASS 2A OR 2B REMOVE BURRS & SHARP EDGES .020 MAX. MACH. FILET RADIUS .020 R MAX. MACH. SURF. FLAT WITHIN .001 IN/IN OTHER SURF. FLAT WITHIN .005 IN/IN ELECTRICAL DWG DESIGNATIONS REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIG- NATION OR BOTH.		CHK		MAT'L	
		ENG		FINISH	
		APP			
		NEXT ASSY			
SIZE		D		TMX-12	
SCALE		NONE		SH 1 OF 3	

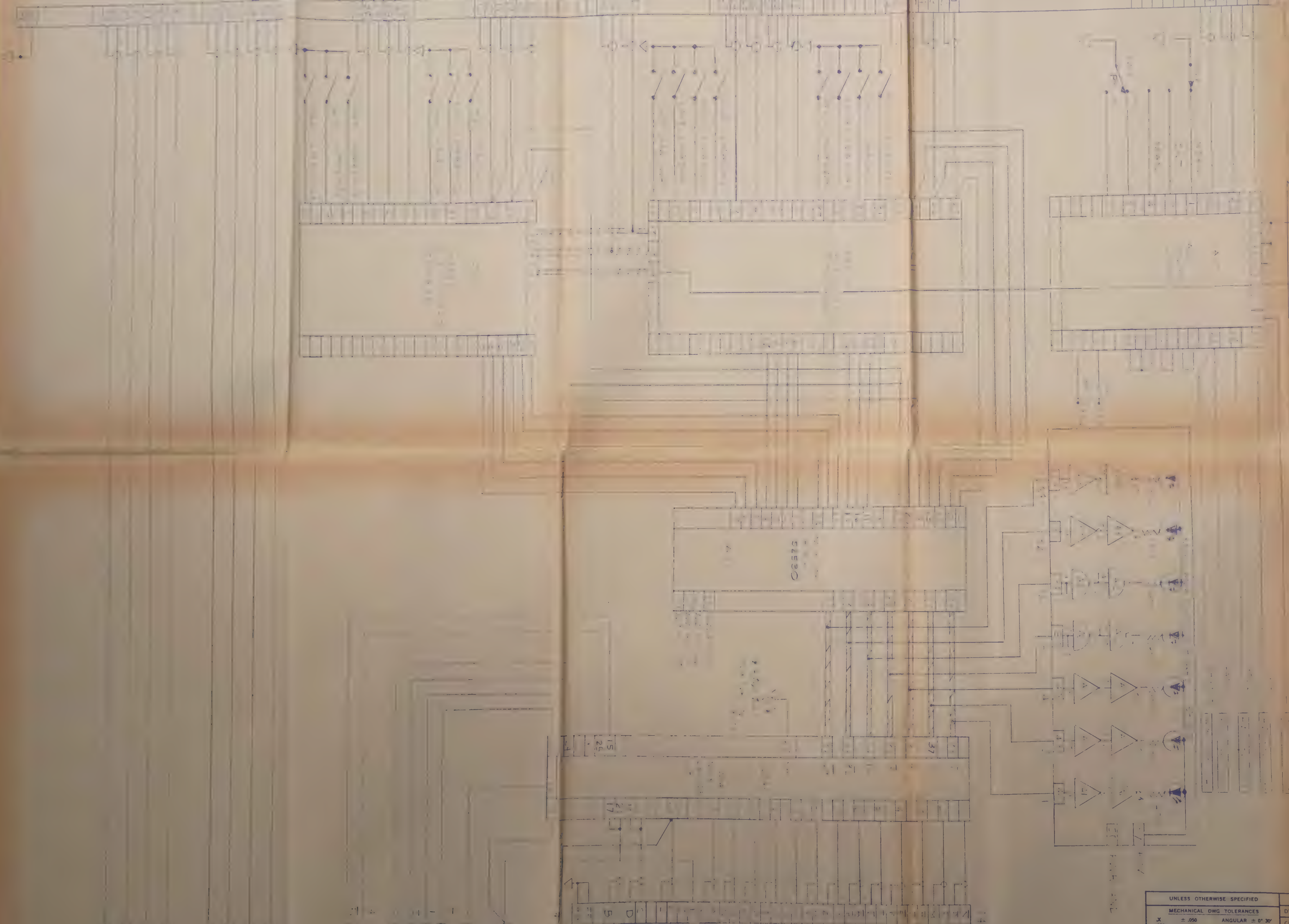
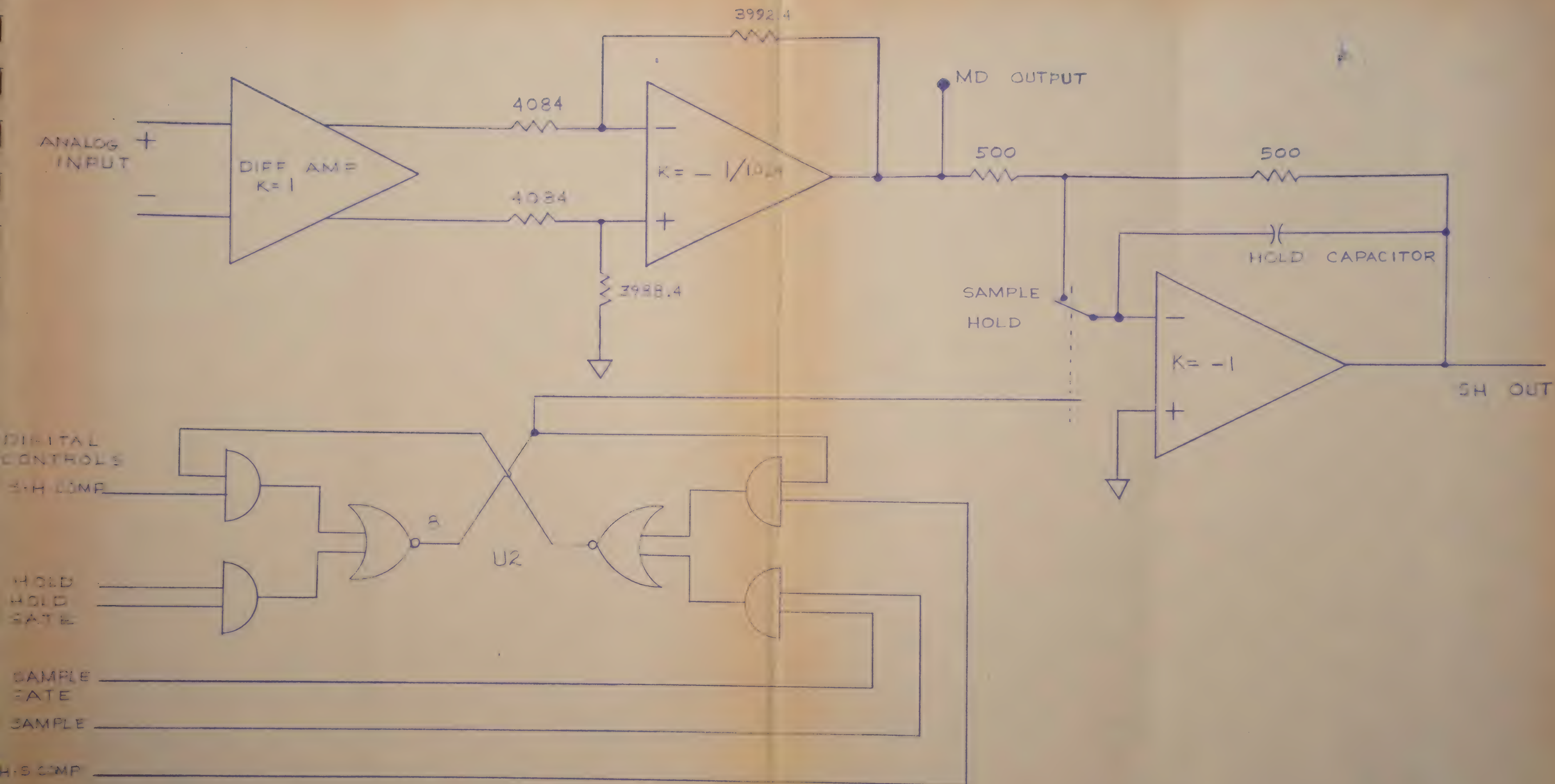


FIGURE TMX-19

TWO'S COMPLEMENT-TO- THEORETICAL INPUT VOLTAGE CONVERSION.

ANALOG INPUT = +/- 10.2400 VOLTS (FULL-SCALE)
 RESOLUTION = 15 BITS INCLUDING SIGN.

TWO'S COMPLEMENT NUMBER	THEORETICAL INPUT	ACTUAL INPUT
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	+ 10.2394 VOLTS	_____
0 1 1 1 1 1 1 1 1 1 1 1 1 1 0	+ 10.2387 VOLTS	_____
0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	+ 9.6000 VOLTS	_____
0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	+ 8.9600 VOLTS	_____
0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	+ 7.6800 VOLTS	_____
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	+ 5.1200 VOLTS	_____
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	+ 1.2800 VOLTS	_____
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	+ 0.6400 VOLTS	_____
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	+ 0.0012 VOLTS	_____
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	+ 0.0006 VOLTS	_____
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	+ 0.0000 VOLTS	_____
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 0.0006 VOLTS	_____
1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	- 0.6400 VOLTS	_____
1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	- 1.2800 VOLTS	_____
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	- 2.5600 VOLTS	_____
1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	- 5.1200 VOLTS	_____
1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	- 7.6800 VOLTS	_____
1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	- 8.9600 VOLTS	_____
1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	- 9.6000 VOLTS	_____
1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	- 10.2387 VOLTS	_____
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	- 10.2394 VOLTS	_____
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	- 10.2400 VOLTS	_____



BLOCK DIAGRAM SAMPLE-AND-HOLD 52380-14

TMX-21

SD7903.10

*** ANALOG INPUT CONNECTIONS ***

THIS SYSTEM USES A DIFFERENTIAL MULTIPLEXER INPUT CHANNELS WHICH, IN TURN, USE DIFFERENT INPUT TERMINATIONS. ALL SIGNALS, EVEN DIFFERENTIAL INPUTS, MUST BE REFERENCED TO ANALOG GROUND. DIFFERENTIAL INPUTS WILL NOT WORK PROPERLY WITH A SIGNAL FROM "HI" TO "LO" WITHOUT THIS REFERENCE. IF NEITHER INPUT IS CONNECTED TO ANALOG GROUND, THE OUTPUT WILL BE NO GREATER THAN 10 MEGOHMS TO GROUND.

*** EXAMPLE ***



THE OUTPUT WILL BE PROPORTIONAL TO THE DIFFERENCE BETWEEN "V1" AND "V2". IF EITHER INPUT IS NOT REFERENCED TO ANALOG GROUND, THE OUTPUT WILL NOT BE PREDICTABLE.

THE TYPES OF INPUT TERMINATIONS IN THIS SYSTEM ARE AS FOLLOWS:

CH0 >>>>> CH3

DIFFERENTIAL

REAR PANEL
CONNECTOR



THESE FOUR CHANNELS TAKE EXCEPTION TO THE RULE LISTING FOR DIFFERENTIAL INPUTS. IN THAT THE SHIELDING IS USED TO GROUND AND NOT BOUND AS IS COMMON WITH DIFFERENTIAL INPUTS. THEREFORE THESE CHANNELS WILL HAVE A GROUND REFERENCE IF THE SHIELD IS CONNECTED TO THE SOURCE. IF NOT A GROUND REFERENCE IS REQUIRED.

CH4 >>>>> CH19

SINGLE-ENDED

REAR PANEL
CONNECTOR

4 CH MUX
CARD



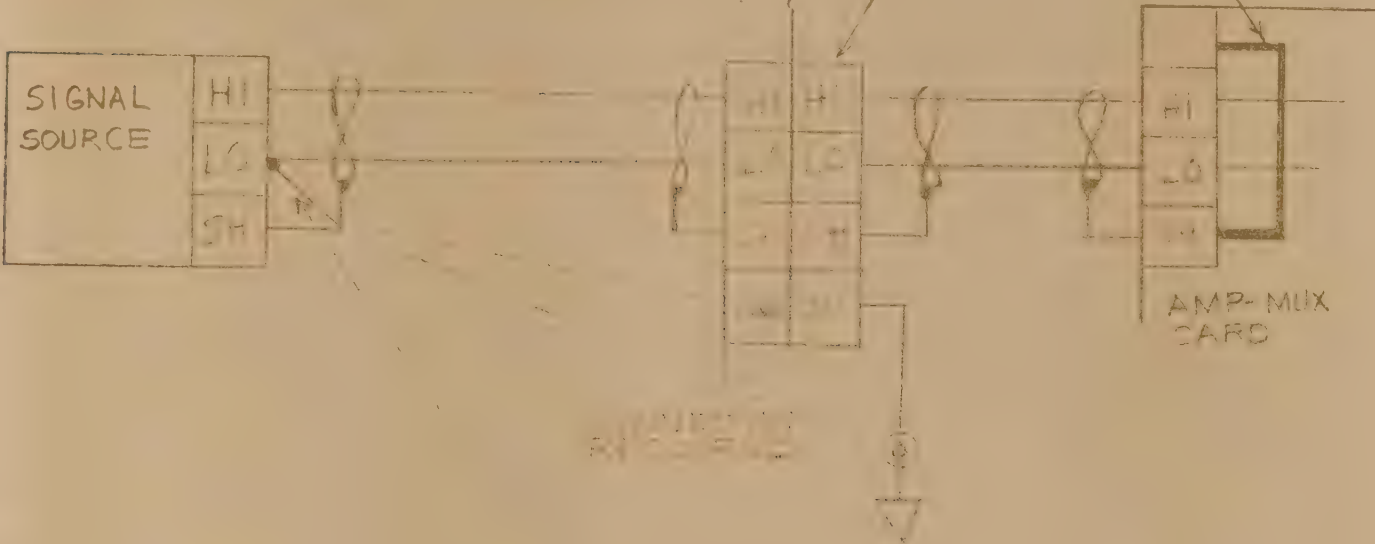
ANALOG
64K

CH20 >>>>>> CH29

DIFFERENTIAL

REAR PANEL
CONNECTOR

INPUT GUARD
NOT TIED
TO GND



SUGGESTED CONNECTION OF
SHIELD TO INPUT LO OR
COMMON MODE SOURCE
@ INPUT

ANA GND STUD

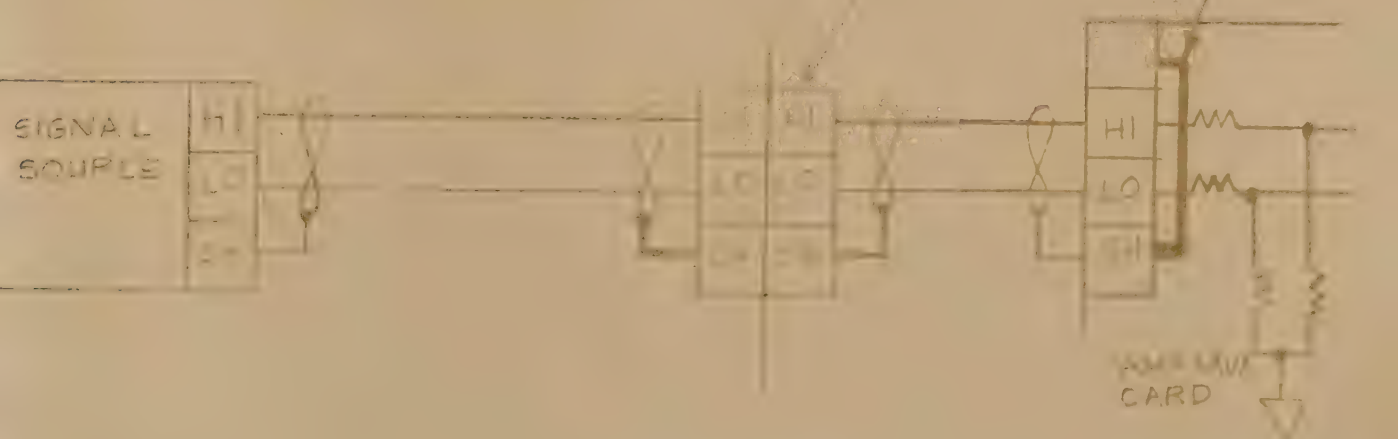
GND REF REQUIRED.

CH30 >>>>>> CH55

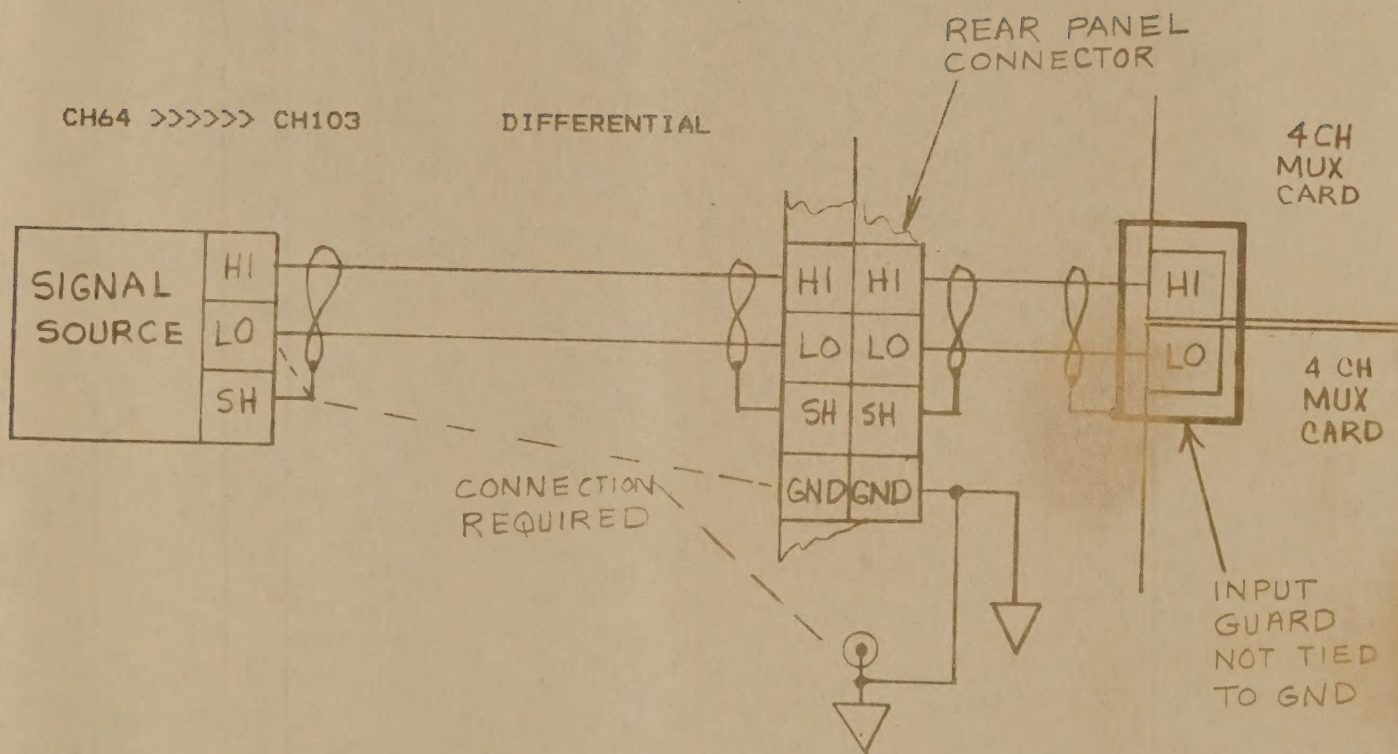
DIFFERENTIAL

REAR PANEL
CONNECTOR

INPUT GUARD
NOT TIED
TO GND

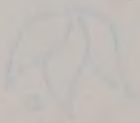
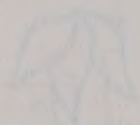


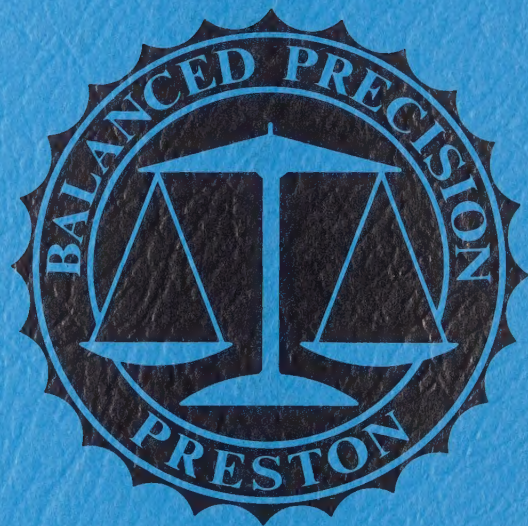
THESE CHANNELS HAVE INPUT ATTENUATORS WHICH REFERENCE INPUTS TO GND



GND REF REQUIRED.

NOTE: CH56 >>>>> 64 ADDRESSES ARE NOT USED , AND ARE INVALID CODES.





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